SLA-1500-SOM Hardware Development Kit

PN: ICD-SLA-1500-SOM

DATE: July 19, 2017

Hood River, OR 97031

Overview

This document describes the integration of the SLA-1500-SOM with the SLA-1500-OEM board. The SLA-1500-OEM can be used as a reference design for customers who plan to integrate the SLA-1500-SOM directly onto their own board. Designing in the SLA-1500-SOM can potentially save weight and power by reducing duplication of common circuits such as power and communication. Additional weight can be reduced by removing the need for cables and connectors. Additional simplifications to heat sink design and other mechanical considerations can be achieved by integrating the SLA-1500-SOM.

Current production release of the SLA-1500-OEM hardware is Revision E (REV E). This Hardware Development Kit (HDK) includes the latest design changes that we think will help customers on their path to integrating the SLA-1500-SOM.

For a more complete design you may also be interested in many of our additional adapter boards which provide designs for connecting to a number of different camera interfaces such as SONY, Camera Link, Hitachi, HDMI, and many thermal cameras. Schematics and mechanical models are available from SightLine.

There are also many Engineering Application Notes (EANs) available from SightLine regarding FPGA programming, digital video formatting, serial and Ethernet communication, and troubleshooting. Please check the SightLine web site to review the latest materials available.

What you will need...

Filename	Purpose
ICD-SLA-1500-SOM.pdf	This document.
SLA-1500-OEM-_RevE_Model.step	3D Step Model of SLA-1500-SOM and SLA-1500-OEM
SLA-1500-OEM_Schematic_RevE.PDF	Schematic for the SLA-1500-OEM
SLA1500-OEM_BOM_RevE_MasterCopy.xls	Bill of Materials Spreadsheet
SightLineProductLicense.pdf	Describes summary of licensing of these and other SightLine materials.

SLA-1500-SOM

The SLA-1500-SOM is a LogicPD DM3730 Torpedo™ SOM (SOMDM3730-20-1780AGIR). As a first step, download and review all the LogicPD design guidelines and support material for the SOM.

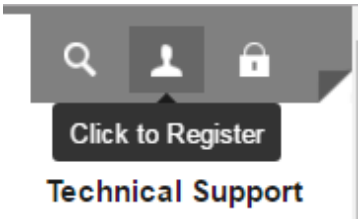
Design Recommendations

- Provide access to the microSD card as this is ued to firmware upgrade the unit and for onboard storage.
- Proved access to Serial Port 0 (/dev/ttyO0) for debug and command and control
- Provide clearly marked silk screen to ensure correct orientation when assembling the SOM onto your carrier board
- LogicPD also provides a design review list

Instructions for Downloading

Accessing the documentation should be very simple. Keep in mind that 3rd party web sites may change, so these instructions should be used as guidance only; the actual procedure may be different.

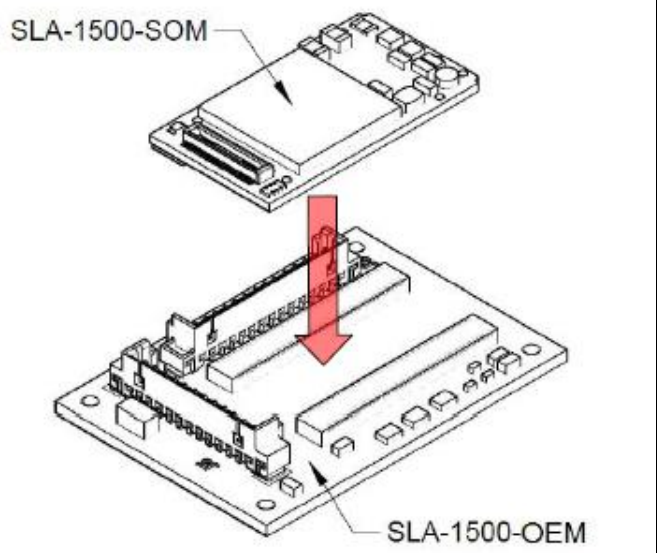
1. At the top of the LogicPD web site, click the "Register" button.

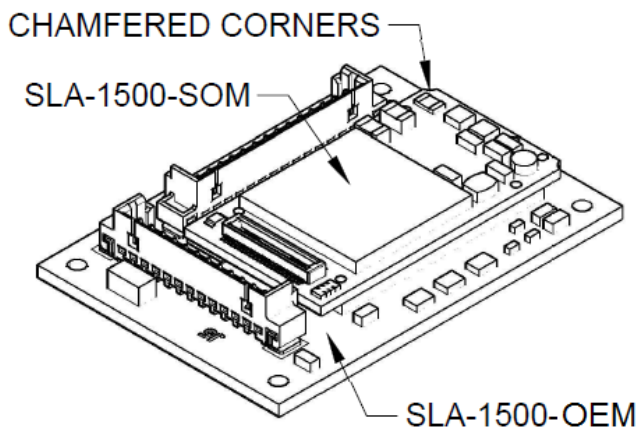


2. You will prompted for basic information such as Name, Company, Business Address, and email.
3. The web site will then send you an email to confirm your identity.
4. Once complete you should have access to all the relevant documentation. No additional registration information was required.

Please email us if there are documents that you cannot access.

SLA-1500-OEM





Shows orientation of SLA-1500-SOM relative to SLA-1500-OEM.

The SLA-1500-OEM is a breakout board for the SLA-1500-SOM that provides power, analog video decoder, Ethernet PHY, serial port access, and a MicroSD card slot. Please review the SLA-1500-OEM schematic for details about the design. The data below is a summary of connectors that can be considered an outline of the major interfaces that you will likely integrate to directly on your board.

Connector J3: Analog Video, Power, Serial, Ethernet

Pin	Signal	Description	Pin	Signal	Description
1	Vin	Analog Video Input	8	5VDC	SOM: 4.5 - 6.0 VDC (5 VDC nom). **Note:** Some adaptor boards are limited to 6.0 V max.
2	AGND		9	5VDC	
3	Vout	Analog Video Output	10	DGND	
4	AGND		11	RX-	10/100BaseT Ethernet
5	TXA	3.3V Serial	12	RX+	
6	RXA		13	TX+	
7	DGND		14	TX-	

Connector J4: Digital Camera, Serial, Power (DEFAULT)

This connector is designed to allow the SLA-1500-OEM to mate with the FLIR TAU 640. However, this is a generic camera input supporting up to 12-bits video data. The SLA-1500-SOM can accept many types of digital video input. For optimal processing performance we recommend the height and width of the image be a multiple of 16.

NOTE: VIOSEL (PIN 46) can be set to either 1.8V or 3.3V.

Comment	Signal Level	Signal	Pin	Pin	Signal	Signal Level	Comment
Serial from camera	VIOSEL	RXB	1	2	TXB	VIOSEL	Serial to camera
FPGA Application Dependent	VIOSEL	CAMXCLKA	3	4	CAMXCLKB	VIOSEL	FPGA Application Dependent
		DGND	5	6	DGND		
	VIOSEL	I2C3SCL	7	8	I2C3SDA	VIOSEL	
Level Shifted GPIO175	VIOSEL	CAMIRQ	9	10	CAMFLD	VIOSEL	FPGA Application Dependent
FPGA Application Dependent	VIOSEL	CAMVS	11	12	CAMHS	VIOSEL	FPGA Application Dependent
Level Shifted GPIO174	VIOSEL	CAMSYSEN	13	14	CAMSTROBE	VIOSEL	Level Shifted GPIO173
	VIOSEL	RXC	15	16	TXC	VIOSEL	
		DGND	17	18	TAUDET*		Grounded to disable pins 9-16
WH/BL Hot Out to Camera	3.3V	DISC0	19	20	CAMD13	VIOSEL	FPGA Application Dependent
FPGA Application Dependent	VIOSEL	EXTSYNC	21	22	CAMD12	VIOSEL	FPGA Application Dependent
FPGA Application Dependent	VIOSEL	CAMD11	23	24	CAMD10	VIOSEL	FPGA Application Dependent
FPGA Application Dependent	VIOSEL	CAMD09	25	26	CAMD08	VIOSEL	FPGA Application Dependent
		DGND	27	28	DGND		
FPGA Application Dependent	VIOSEL	CAMD07	29	30	CAMD06	VIOSEL	FPGA Application Dependent
FPGA Application Dependent	VIOSEL	CAMD05	31	32	CAMD04	VIOSEL	FPGA Application Dependent
FPGA Application Dependent	VIOSEL	CAMD03	33	34	CAMD02	VIOSEL	FPGA Application Dependent
FPGA Application Dependent	VIOSEL	CAMD01	35	36	CAMD00	VIOSEL	FPGA Application Dependent
		DGND	37	38	DGND		
FPGA Application Dependent	VIOSEL	CAMPCLK	39	40	CAMWEN	VIOSEL	Level Shifted GPIO172
		DGND	41	42	DGND		
		VIDEOIN2	43	44	AGND		
		DGND	45	46	VIOSEL		Sets I/O voltage (1.8 or 3.3)
Power return		DGND	47	48	VIN		5 V to camera
Power return		DGND	49	50	VIN		5 V to camera
Hirose 50 pin connector							

Connector J4: GPIO, Serial, Power (Alternate Configuration)

Signal Level	Name	Pin	Pin	Name	Signal Level	Signal Level	Name	Pin	Pin	Name	Signal Level
VIOSEL	RXB	1	2	TXB	VIOSEL		DGND	27	28	DGND	
		3	4					29	30		
	DGND	5	6	DGND				31	32		
VIOSEL	I2C SCL	7	8	I2C SDA	VIOSEL			33	34		
	GPIO175	9	10					35	36		
		11	12				DGND	37	38	DGND	
VIOSEL	GPIO174	13	14	GPIO173	VIOSEL			39	40	GPIO172	VIOSEL
VIOSEL	RXC	15	16	TXC	VIOSEL		DGND	41	42	DGND	
	DGND	17	18				VideoIn1	43	44	AGND	
3.3V	GPIO178	19	20				DGND	45	46	VIOSEL	
		21	22				DGND	47	48	+5V	
		23	24				DGND	49	50	+5V	
		25	26								

NOTE: if not specified, pin should be left as No Connect [NC]
NOTE: Alternate configurations may be available.

Connector J5: FPGA JTAG

Use with SLA-CAB-1512 and SLA-1500-AB board.

Pin	Signal	Description	Pin	Signal	Description
1	Internal Use Only		7	TMS	
2			8	TDI	
3			9	VJTAG	
4			10	TRST	
5	DGND		11	TDO	
6	TCK		12	VPUMP	

Power

Connector/Pin	Name	Range
J4 Pin 46	VIOSEL	1.8, 2.5V, 3.3V
J4 Pin 48 & 50	P5V	4.5 – 6.5V
J3 Pin 8 & 9	P5V	4.5 – 6.5V

NOTE: Apply 5V to either J3 (Pin 8 & 9) or J4 (Pin 48 & 50). Do not apply power to both.

NOTE: Do not exceed 3.3V on VIOSEL

LEDS

Label	Description
D1	Power Indicator
D2	GPIO179
D3	Network Status

UARTS

RXn/TXn	Reference Voltage	Connector	Linux	Name	Common Use
A	3.3V	J3:P5/6	/dev/ttyO0	Serial Port 0	Command and Control
B	VIOSEL (J4:P46)	J4:P1/2	/dev/ttyO2	Serial Port 2	User Defined or Camera communication
C	VIOSEL (J4:P46)	J4:P15/16	/dev/ttyO1	Serial Port 1	User Defined or Lens Control

Test Points

Label	Description	Label	Description
TP1	Ground	TP3	FPGA Pin B9
TP2	3.3V	TP4	FPGA Pin C8

GPIO

Label	Reference Voltage	Description/ Location	Label	Reference Voltage	Description/Location
GPIO127	GROUND		GPIO174	VIOSEL	J4 Pin 13 (CAMSYSEN)
GPIO129		LAN9221 Pin 43 (IRQ)	GPIO175	VIOSEL	J4 Pin 9 (CAMIRQ)
GPIO171		FPGA A9	GPIO178	3.3V	J4 Pin 19 (DISC0)
GPIO172	VIOSEL	J4 Pin 40 (CAMEN)	GPIO179	3.3V	LED D2
GPIO173	VIOSEL	J4 Pin 14 (CAMSTROBE)			

Layout Notes

Critical Placement	• Bypass capacitors shown near U1 • C20 and C24 near U6 • X1 near U2 • Discrete components (except for R30, R1, R2) near U2 • X2 near U3 • Discrete components near U3 • Discrete components (except for R35, C45, C46, C52) near U5
Controlled Impedance	If any of these traces are less than 0.5”, then controlled impedance is not required.
	The following traces are 75 Ohm, single ended over analog ground: • J2-64 to J3-3 • J3-1 to R3 • J4-43 to R33
	The following traces are 90 Ohm, differential pairs over digital ground: • U3-45 to C37 and C37 to J3-13 • U3-44 to C38 and C38 to J3-14 • U3-48 to C39 and C39 to J3-12 • U3-47 to C40 and C40 to J3-11
	Note: R13, R18, R19 and R20 should be placed so they can be connected to the corresponding controlled impedance traces with very short stubs or vias.
High Current	• J3-7 and J3-10 to DGND up to 2 amps • J3-8 and J3-9 to Q1-1 and Q1-3 up to 2 amps • Q1-5 to U5-15, U5-1 and U5-2 up to 2 amps • U5-10, U5-11 and U5-12 to L1 up to 2 amps • U5-3, U5-4, U5-5 and U5-17 (thermal pad) to DGND up to 2 amps • L1 to C28 and C29 up to 2 amps • C28 and C29 to DGND up to 2 amps • L1 to L4 up to 1 amp • Q1-5 to J5-1 up to 1 amp • J5-5 to DGND up to 1 amp

Video Signals from FPGA to DSP

DSP input

- 12-bit possible inputs - we only use 8 bits (CSID0 → CSID7)
- Digital Cameras → HSync, VSync, Pixel Clock - rising edge (CSIHS, CSIVS, CSIPCLK)
- We don't use Field.
- Analog video comes in as BT.656 (8-bit data and pixel clock only)
- Maximum pixel clock is 148.5 MHz.
  - For a YUV camera, this means maximum camera pixel clock is 74.25 MHz
  - Camera pixel clock must be doubled (as there are 2x 8 bit values per pixel) before it can go to the DSP
  - For 8-bit gray-scale cameras, the maximum camera pixel clock rate is 74.25 MHz.
    - this is due to Linux driver "bridge" - this can be changed in the future
  - For 14-bit gray-scale camera the maximum camera pixel clock rate is 74.25 MHz. (because it must be doubled for 2x 8-bit outputs)
- Typically, our processing is more consistent at 30 Hz frame rates
  - We can accept 60 Hz video, and "frame step" the video down to 30 fps when acquiring frames.

Camera types (Analog, YUV, Digital, Embedded Sync)

- Analog video input is BT.656 (8-bits of data and a pixel clock)
- YUV Color cameras
  - 8 bit values
  - UYVY order, (PrYPbY) - 1 clock cycle per element (4 elements == 2 pixels) This is 4:2:2
- Digital grayscale cameras (and Camera Link)
  - 8-bit values - one pixel clock per value
  - 14-bit values - the DM3730 is little endian. High 2 bits are 0. So low byte followed by high byte (with upper 2 bits == 0)
  - Currently our autogain only supports 14-bit inputs, this may change in future firmware
  - For a 16-bit Camera Link input, we shift down by 2-bits (for now)
- Embedded Sync Digital cameras. (BT.1120)
  - FPGA decodes sync signals and provides VSync, HSync to DSP
- Embedded Sync BT.656 cameras - can be acquired by DSP with 8-bit data, pixel clock

Notes

- In practice, we have found the delaying the pixel data (D0 → D7) relative to the rising edge of the pixel clock is necessary to eliminate bit errors ("sparkles in video")
- Generally, this delay has been about 4 nSec.
- This may be just an issue with our FPGA timing.

SightLine Product Export Controls

Exports of SightLine products are governed by the US Department of Commerce, Export Administration Regulations (EAR); classification is ECCN 4A994. The export summary sheet located on the support/documentation page of our website outlines customers responsibilities and applicable rules. SightLine Applications takes export controls seriously and works to stay compliant with all export rules.

Copyright and Use Agreement

FILES

Additional files such as 3D models, Schematics, Gerbers, etc. may be available for some products. Contact your Sales Engineer for more information.

ERRATA

Please contact your Sales Engineer often as new versions of the product (new schematics, etc.) may be available.

KNOWN ISSUES

The SLA-1500-OEM (REV E) serial receive pin (J3 Pin 6) should be driven to 3.3V when not in use. This will prevent the SLA-1500-OEM from detecting an unintentional interrupt during power-up.

Contacts

Web: sightlineapplications.com

Sales: sales@sightlineapplications.com

Support: support@sightlineapplications.com

Phone: +1 (541) 716-5137