SightLine APPLICATIONS

ICD-3000-OEM

PN: ICD-3000-OEM

11/9/2018

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Alerts

The following notifications are used throughout the document to help identify important safety and setup information to the user:

⚠ **CAUTION:** Alerts to a potential hazard that may result in personal injury, or an unsafe practice that causes damage to the equipment if not avoided.

ⓘ **IMPORTANT:** Identifies crucial information that is important to setup and configuration procedures.

Used to emphasize points or reminds the user of something. Supplementary information that aids in the use or understanding of the equipment or subject that is not critical to system use.

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Revision History

Date	Description
10/31/2018	Added 3000-OEM Thermal Pad drawing and pad table to Gap Pads section.
10/25/2018	Add Notes on J2: Video Output signals.
9/25/2018	Updated information on altering the corners of the PCB board.
9/10/2018	Added supply voltage level compatibility statement for camera boards.
8/23/2018	Added VOUT supported resolutions
8/22/2018	Update to Video Input Port description
7/3/2018	Updated LED Summary section.
6/12/2018	Updated adapter ID for FPC board.
5/22/2018	Added notes explaining D2/D3 LED functions to LED Summary section.
3/9/2018	Highlighted that input voltage can be passed to camera through adapter board. Added details on Port ID and Board ID.
2/14/2017	Analog out is incompatible with Digital output (Vout, HDMI).
12/20/2017	Syntax updates. Added notes on thermal and magnetics.
12/14/2017	Clarified notes on generic adapter ID 0xD.
11/9/2017	Updated document to new format and edited for clarity. Created new ICD document for 3000-OEM adapter boards. See ICD-3000-Adapters.
7/28/2017	Add notes on generic adapter ID, GPIO pin and reset/power-down lines.
5/18/2017	Add notes on minimum vertical blanking.
4/28/2017	Add in video timing diagram for 1080P as an example.
4/27/2017	Correct HDVPSS timing information chapter (8.10.1).

4/26/2017	Add detailed information on synchronization edges, maximum input pixel clock, reference to TI HDVPSS input timing documentation.
4/24/2017	Add section detailing how to measure blanking.
4/22/2017	Add section on synchronization signals and blanking.
3/15/2017	Fix error in supported data formats, should by YCbCr.
2/16/2017	Add section on supported camera data formats.
2/7/2017	Add Port A and Port B data bit locations to VIP ports.
1/25/2017	Adding information for rounding the corners, embedded Ethernet, update HDSDI-IN image and connector descriptions. Add: 3000-CL board.
1/10/2017	Specify grayscale input data bit locations. Add notes on I2C Linux bus numbering.
1/6/2017	Change generic adapter ID = 0xD. Note that adapter ID = 0 will result in no video acquisition.
10/24/2016	Mod: Input Mezzanine Board Address table to include more information when a board is not connected. Identify IDs that are reserved.
9/26/2016	Add: SLA-3000-HDMI board.
9/9/2016	Add: Temperature sensor information.
8/1/2016	Updated PRELIMINARY Junction-to-Case Thermal Resistance (Theta-JC) section with new image, notes, and part number.
5/10/2016	Add notes on grayscale support.
2/4/2016	Add notes regarding serial port voltage levels and Ethernet 10/100.
1/26/2016	Add: section on safe device handling and thermal management. Added: 3000-USB section
11/13/2015	Added other adapter boards.
10/6/2015	Update bideo formats, LED summary, test points, camera naming convention, table captions
9/8/2015	Updated tables for J3 and J4. Add SLA-3000-HDSDI-IN (REV B) photo.
6/30/2015	Insert ToC, numerous table and illustration captions, and formatting changes. Added design checklist. Renamed SLA-3000-MAIN to 3000-IO.
2/2/2015	Formatting, photo changes.
5/27/2014	Formatting, address update.
5/22/2014	Updated video input connector tables, voltage level, description, mezzanine ID.

1 Overview

Describes power requirements, thermal management, interface specifications, and connector pin-outs for the 3000-OEM video processing board.

1.1 Associated Documents

EAN-Startup Guide 3000-OEM: Describes steps for connecting, configuring, and testing the 3000-OEM video processing board on the 3000-IO interface board.

EAN-File Recording: Describes how to record video or snap shots to either the onboard microSD card or to an external FTP drive.

ICD-3000 Adapter Boards: Describes power requirements, thermal management, interface specifications, and connector pin-outs for the 3000-OEM associated camera interface boards.

Interface Command and Control (IDD): Describes the native communications protocol used by the SightLine Applications product line. The IDD is also available as a local download on the Software Download page.

EAN-Panel Plus User Guide: Provides descriptions of all the settings in the Panel Plus application. (Located in the Panel Plus application in the *Help* menu.)

1.2 Sightline Software Requirements

Panel Plus software and firmware versions:

3000-OEM requires Panel Plus and Firmware 2.23.0 and higher.

3000-OEM (REV C) requires Panel Plus and firmware 2.24.xx and higher.

ⓘ **IMPORTANT:** The Panel Plus software version should match the firmware version running on the board.

2 Safe Device Handling

△ **CAUTION:** To prevent damage to hardware boards, use a conductive wrist strap attached to a good earth ground. Before picking up an ESD sensitive electronic component, discharge built up static by touching a grounded bare metal surface or approved antistatic mat.

3 3000-OEM Overview

The 3000-OEM has four connectors on the bottom side that are designed for board-to-board connectivity. The connectors are: Main (Power, Ethernet, Serial, HDMI and analog output), Input Channels 0 and 1 (Digital Video In, power out, and serial), and the Optional Output Video (Digital Video Out).

Figure 1: 3000-OEM Overview

3.1 3000-OEM Specifications

Revision: C (green)

Dimensions: 3.465 in x 1.969 in (88 mm x 50 mm)

Weight: 38 grams

Voltage: 5 - 15V DC (12V Nominal)

Power: < 10 Watts with 12V nominal DC input

Drawing: 3000-OEM Drawing Rev C

3000-OEM Drawing Rev B

3000-OEM Assembly

STEP File: 3000-OEM Rev C STEP

3000-OEM Rev B STEP

All 300-OEM board mounting holes support M1.6 screws.

IMPORTANT: The supply voltage level must be compatible with camera adapter board and connected cameras. For example, the 3000-Sony camera adapter board passes supply voltage directly to the attached camera. A Sony EH series camera can only support 6V - 12V, which would limit the supply voltage of the 3000-OEM to this range.

3.2 Hardware Revisions

Board Revision	Changes
Rev C	Adds a power control circuit to allow integrators to turn off the C66 DSP processor.
Rev B	Initial production release.

3.3 Interface Protocol

The 3000-OEM shares the same interface protocol as other SLA video processing boards. The protocol is a packet-based command and control interface. There is an ARM core on the DM8148 that is only lightly utilized in the SLA implementation. This provides customers with a processor to implement other processing functions or protocol conversions (allows communications via a customer's proprietary protocol).

3.4 Functional Block Diagram

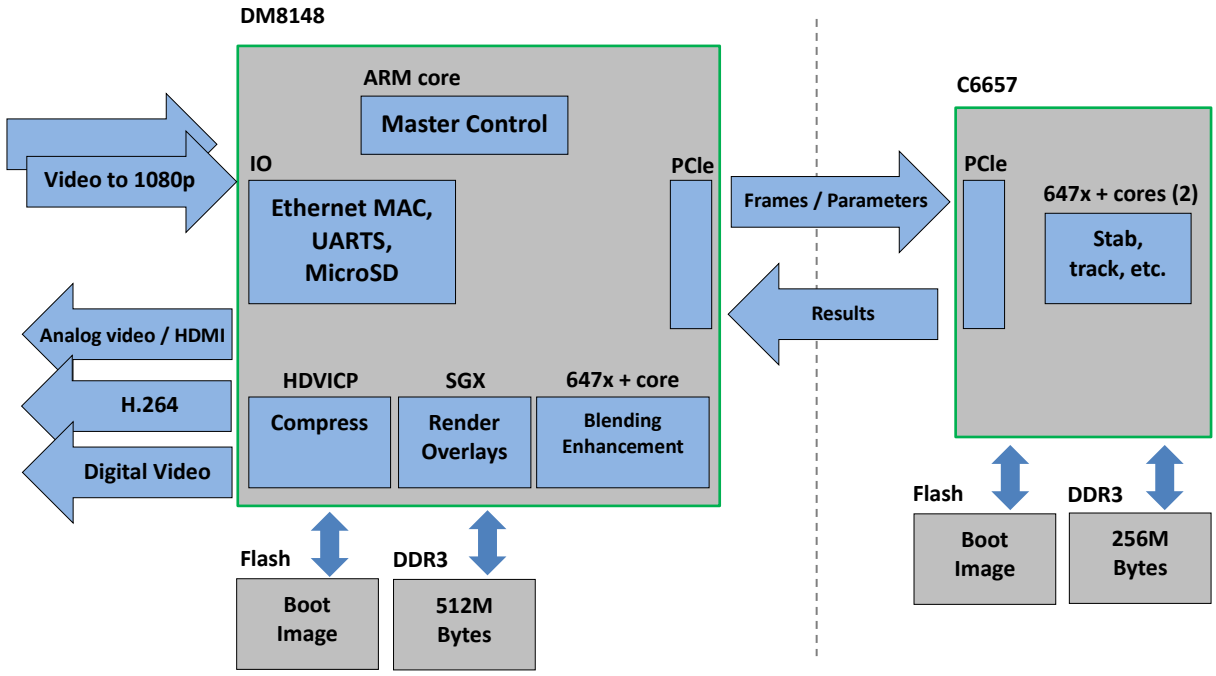

Figure 2: 3000-OEM Hardware Block Diagram

3.5 Design Checklist

- ✓ Provide a sufficient heat sink for the DSP and other major components
- ✓ Expose serial port 0 to connector for debugging
- ✓ Use serial port 1 for command and control, otherwise use Ethernet port. Alternately serial port 2, 3, 4[1] can also be used for command and control
- ✓ Expose Ethernet port for debug, command and control, and firmware update capability
- ✓ Expose analog video output and ground for debugging
- ✓ Provide test points for all serial port signals
- ✓ Expose test point for video sync signals
- ✓ Expose microSD card signals for failsafe recovery (future improvements)
- ✓ All serial ports are 3.3V TTL levels (unless otherwise noted)

1 This feature may not be available for all software releases.

3.6 PCB Corner Alternations

The corners of the 3000-OEM board can be removed or rounded off if needed. A needle file works best for this procedure.

ⓘ **IMPORTANT:** Considerable care should be taken when removing or rounding off the corners to prevent damage to the board.

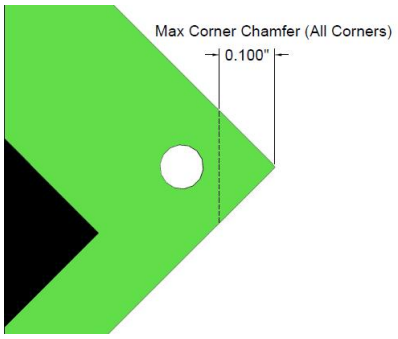

Figure 3: Corner Alternations

4 Thermal Management

4.1 Heatsink Guidelines

The component temp range is -40°C to 85°C. All hardware uses some form of mechanical heatsink. The 3000-OEM typical power consumption is less than 10W @ 12V. Most of the power is used by the two DSP chips. A new single DSP mode is now available that reduces power consumption to approximately 6W, but it has some functional limitations.

A large heatsink to facilitate bench and early testing is provided by SightLine. It supports convective cooling when there is airflow.

ⓘ **IMPORTANT:** The large heatsink is not intended for long term vehicle integration use.

Most customers design a heatsink in conjunction with their system integration effort that provides a direct conducted path to a significant thermal mass (typically the wall of a gimbal or housing). Others use active cooling (fans) as part of the design.

STEP files for the heatsink interface are available from SightLine that can help with heatsink design and integration.

4.2 Gap Filler (Thermal Grease)

When possible use some form of thermally conductive liquid gap filling material such as Artic Silver rather than an adhesive. Do not use thermal grease in conjunction with gap pads.

4.3 Gap Pads

Use some form of thermally conductive material for filling gaps between the hot components and the heat sink. Examples such as the Bergquist VO Ultra Soft are recommended. Do not use gap pads in conjunction with thermal grease.

Table 1: Thermal Pads

Thermal Pads	Manufactures PN	Description	MFG
SLA-PAD-010	GP1500R-0.010-02-0816	Thermal Pad Black 1.0 X 1.0 x 0.010 - inch Tacky - Both Sides	Berqquist
SLA-PAD-125	GPVOUS-0.125-00-0816	Thermal Pad Pink 0.250 X 0.250 x 0.125 - inch	Berqquist
SLA-PAD-020	GPVOUS-0.020-00-0816	Thermal Pad Pink 0.75 X 0.75 x 0.020 - inch	Berqquist

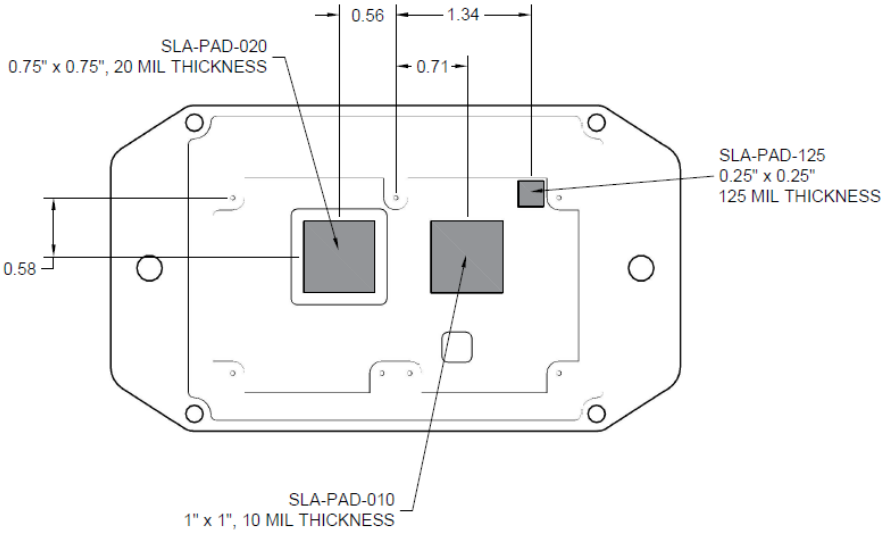

Figure 4: 3000-OEM Thermal Pad Placement

See 3000-OEM Assembly drawing for additional information.

4.4 Preliminary Junction-to-Case Thermal Resistance (Theta-JC)

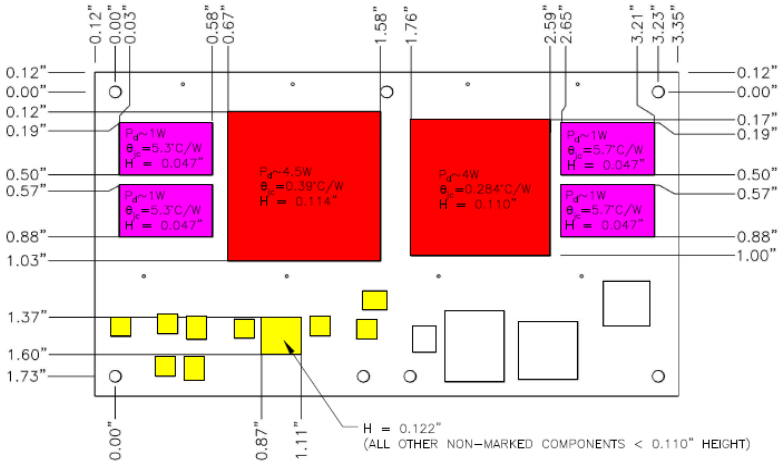

Figure 5: 3000-OEM Thermal Drawing (REV B3)

Drawing notes:

- All dimensions in inches.
- Devices in yellow dissipate less than 1/4W per IC.
- All height (H) values are estimates. Since there is a lot of variation, use gap pads to make good contact.

Table 2: Component Thermal Resistance Specifications

Description	Manufactures PN	Temp Range	Theta-JC
DM8148	TMS320DM8148CCYEA0	-40° to 105°C	0.39 C/W
ISSI memory (for 8148)	IS43TR16128A-15HBLI	-40° to 95°C	5.3 C/W
C6657	TMS320C6657CZHA25	-40° to 100°C	0.284 C/W
Micron memory (for 6657)	MT41J64M16JT-15E IT:G	-40° to 95°C	5.7 C/W

4.5 Temperature Sensor - U4

Temperature is read by on onboard NXP LM75BGD. The temperature is queried once per second. The temperature can be requested by sending the Get Version (0x00) command. The sensor is located on the bottom of the board.

To get an accurate reading, the U4 sensor chip should share the same heatsink as the DSPs.

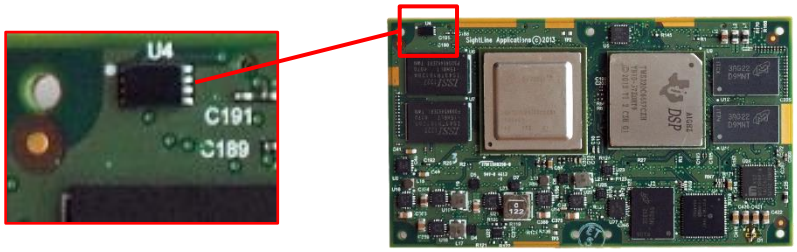

Figure 6: Temperature Sensor

5 Ports, LED, GPIO and Sensors

5.1 LED Summary

Label	Color	Function
D2	Green	Ethernet PHY Activity Indicator (RX / TX)
D3	Amber	Ethernet PHY Link Indicator (Blinking indicates poor link)
D8	Green	GP1[8] Pin W2 [REV D]
D9	Blue	GP1[9] Pin V1 [REV D]

5.2 Serial Port Summary

All serial ports are 3.3V TTL. When using a SightLine mezzanine board with a 3-pin connector, use the CAB-03xx for easy break out to either a pig tail, Molex-to-Molex, or DB-9 connector.

Table 3: 3000-OEM Serial Port Summary

Connector	Name	Device	Notes
J1	Serial Port 0	/dev/ttyO0	Reserve for SightLine debug
J1	Serial Port 1	/dev/ttyO1	
J2	Serial Port 4	/dev/ttyO4	
J3	Serial Port 2	/dev/ttyO2	
J4	Serial Port 3	/dev/ttyO3	

5.3 GPIO Summary

GPIO are used to identify the Input Mezzanine Board Address attached to connectors J2, J3, J4. See current list of IDs in Connector Descriptions.

After bootup, the GPIO may be used for generic Input and Output.

5.4 I2C Port Summary

The I2C Ports available for camera control are on the following ports

Table 4: 3000-OEM I2C Port Summary

Connector	Name	Device	Notes
J2	I2C Bus 0	/dev/i2c-1	Linux I2C bus number is 1
J3	I2C Bus 0	/dev/i2c-1	Linux I2C bus number is 1
J4	I2C Bus 3	/dev/i2c-4	Linux I2C bus number is 4

6 Connector Descriptions

Table 5: Connector Descriptions

Connector	Description
Connector J1: Main	Power, serial port 0, serial port 1, analog video out, HDMI out, 10/100 Ethernet, microSD
Connector J2: Digital Video Output	Digital video out, serial port 4, I2C0
Connector J3: Video Input 0	Digital video in 0, serial port 2, I2C0, GPIO
Connector J4: Video Input 1	Digital video in 1, serial port 3, I2C3, GPIO
P1	JTAG (internal use only)

6.1 Connector J1: Main

Connector: DF12(3.0)-60DS-0.5V(86) Mates with: DF12(3.0)-60DP-0.5V(86)

Table 6: 3000-OEM J1 Pinout

Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	Vin	2	Ground	31	TXPA	32	TXPC
3	Vin	4	Ground	33	TXNA	34	TXNC
5	Vin	6	Ground	35	TXPB	36	TXPD
7	Vin	8	Ground	37	TXNB	38	TXND
9	Vin	10	Ground	39	Ground	40	Ground
11	Vin	12	Ground	41	HDMICLK+	42	HDMID1+
13	Vin	14	Ground	43	HDMICLK-	44	HDMID1-
15	Vin	16	Ground	45	HDMID0+	46	HDMID2+
17	Vin	18	Ground	47	HDMID0-	48	HDMID2-
19	SD0_DAT2	20	SD0_CLK	49	HDMI_SCL	50	HDMI_SDA
21	SD0_CD/DAT3	22	SD0_DAT0	51	Ground	52	Ground
23	SD0_CMD	24	SD0_DAT1	53	+3.3V (out)	54	+3.3V (out)
25	Ground	26	Ground	55	+1.8V (out)	56	+1.8V (out)
27	RX0	28	TX0	57	Video Out 0	58	Video Out 1
29	RX1	30	TX1	59	Video Ground	60	Video Ground

6.1.1 Serial Ports

On connector J1, serial port 0 and serial port 1 (RX0/TX0, RX1/TX1)) are 3.3VTTL. Serial port 0 should be reserved for debugging. Serial port 1 can be used for command and control. TX pins transmit from the 3000-OEM, RX pins receive.

6.1.2 Ethernet

On connector J1, pin 31 through pin 38 represent the Ethernet connection. Currently only 10/100BASE-T has been implemented (Pins 31,33,35,37). 1000BASE-T has not yet been enabled (pins 32, 34, 36, 38).

TXPA/TXNA is sending info from Sightline product., TXPB/TXNB is receiving.

TXPA = TX+

TXNA = TX-

TXPB = RX+

TXNB = RX-

The 3000-OEM uses the embedded Ethernet approach. This consists of 0.033uF capacitors placed in series on the Ethernet lines (AC coupled) onboard. There are no Ethernet magnetics on either the 3000-OEM or the 3000-IO. If the distance is less than a few meters and there is a common ground, there should not be any issues with Ethernet connectivity (even in EMI testing).

ⓘ **IMPORTANT:** If the Ethernet needs to be changed to use external magnetics, the OEM board should be modified by changing the board capacitors (and possibly other passives) to zero-ohm jumpers. Contact Support for modification assistance.

Analog Video output on J1 is incompatible with Digital Video outputs (Vout, Vout1, HDMI). Contact Support for more information.

6.2 Connector J2: Digital Video Output

Connector: DF12(3.0)-60DP-0.5V(86) Mates with: DF12(3.0)-60DS-0.5V(86)

Table 7: 3000-OEM J2 Pinout

Pin	Description	Notes	Pin	Description	Notes
1	VOUT0_CLK	Pixel Clock	2	USB0_ID	
3	Ground		4	USB0_DRVBUS	
5	VOUT0_GYYC_9	Y9	6	VOUT0_GYYC_8	Y8
7	VOUT0_GYYC_7	Y7	8	VOUT0_GYYC_6	Y6
9	VOUT0_GYYC_5	Y5	10	VOUT0_GYYC_4	Y4
11	VOUT0_GYYC_3	Y3	12	VOUT0_GYYC_2	Y2
13	Ground		14	Ground	
15	VOUT0_BSBC_9	CbCr9	16	VOUT0_BSBC_8	CbCr8
17	VOUT0_BSBC_7	CbCr7	18	VOUT0_BSBC_6	CbCr6
19	VOUT0_BSBC_5	CbCr5	20	VOUT0_BSBC_4	CbCr4
21	VOUT0_BSBC_3	CbCr3	22	VOUT0_BSBC_2	CbCr2
23	Ground		24	Ground	
25	VOUT0_RSR_9	0	26	VOUT0_RSR_8	0
27	VOUT0_RSR_7	0	28	VOUT0_RSR_6	0
29	VOUT0_RSR_5	Y1 = 0	30	VOUT0_RSR_4	Y0 = 0
31	VOUT0_RSR_3	CbCr1 = 0	32	VOUT0_RSR_2	CbCr0 = 0
33	Ground		34	Ground	
35	VOUT0_HSYNC	H Sync	36	USB0_DP	
37	VOUT0_VSYNC	V Sync	38	USB0_DM	
39	VOUT0_FLD	Field	40	USB0_VBUSIN	
41	VOUT0_AVID	Active Video (see Active Video Area and Blanking)	42	USB0_CE	
43	Ground		44	Ground	
45	RX4		46	TX4	
47	I2C0_SCL		48	I2C0_SDA	
49	GP0_16		50	GP0_17	
51	GP0_22		52	GP0_23	
53	GP0_24		54	GP0_28	
55	+3.3V (out)		56	+3.3V (out)	
57	Ground		58	Ground	
59	+1.8V (out)		60	+1.8V (out)	

See Video Output for output video format details.

6.3 Connector J3: Video Input 0 (VIN0)

Connector: DF12(3.0)-80DP-0.5V(86) Mates with: DF12(3.0)-80DS-0.5V(86)

In the Notes column in the table below:

Y = luminance **G** = Grayscale **B** = Denotes port B data bits

CbCr = Chrominance **A** = Indicates port A data bits See Color Camera Data Input Signal Locations

Table 8: 3000-OEM J3 Pinout

Pin	Description	Notes	Pin	Description	Notes
2	VIN0_**B**CLK		1	VIN0_**A**CLK	
4	Ground		3	Ground	
6	VIN0_D22		5	VIN0_D23	
8	VIN0_D20		7	VIN0_D21	
10	VIN0_D18		9	VIN0_D19	
12	VIN0_D16		11	VIN0_D17	
14	Ground		13	Ground	
16	VIN0_D14	**Y**6, **G**6, **B**6	15	VIN0_D15	**Y**7, **G**7, **B**7
18	VIN0_D12	**Y**4, **G**4, **B**4	17	VIN0_D13	**Y**5, **G**5, **B**5
20	VIN0_D10	**Y**2, **G**2, **B**2	19	VIN0_D11	**Y**3, **G**3, **B**3
22	VIN0_D8	**Y**0, **G**0, **B**0	21	VIN0_D9	**Y**1, **G**1, **B**1
24	Ground		23	Ground	
26	VIN0_D6	**CbCr**6, **G**14, **A**6	25	VIN0_D7	**CbCr**7, **G**15, **A**7
28	VIN0_D4	**CbCr**4, **G**12, **A**4	27	VIN0_D5	**CbCr**5, **G**13, **A**5
30	VIN0_D2	**CbCr**2, **G**10, **A**2	29	VIN0_D3	**CbCr**3, **G**11, **A**3
32	VIN0_D0	**CbCr**0, **G**8, **A**0	31	VIN0_D1	**CbCr**1, **G**9, **A**1
34	Ground		33	Ground	
36	NC		35	NC[2]	
38	NC		37	NC	
40	NC		39	NC	
42	Port ID (out)	See pin notes below	41	NC	
44	Ground		43	Ground	
46	NC		45	VIN0_HSYNC	
48	NC		47	VIN0_VSYNC	
50	NC		49	VIN0_FLD	
52	NC		51	VIN0_DE	Optional
54	Ground		53	Ground	
56	Passthrough ground		55	Passthrough VIN	See J1
58	Passthrough ground		57	Passthrough VIN	See J1
60	Passthrough ground		59	Passthrough VIN	See J1
62	Passthrough ground		61	Passthrough VIN	See J1
64	Ground		63	Ground	
66	TX2	3.3V TTL	65	RX2	3.3V TTL
68	I2C0_SDA	/dev/i2c-1	67	I2C0_SCL	/dev/i2c-1
70	GP0_8_**ID1**	See below sys/class/gpio/ gpio8	69	GP0_25_**ID0**	See below sys/class/gpio/gpio25
72	GP0_10_**ID3**	sys/class/gpio/gpio10	71	GP0_9_**ID2**	sys/class/gpio/gpio9
74	GP0_15	sys/class/gpio/ gpio15	73	GP0_14	sys/class/gpio/gpio14
76	+3.3V (out)		75	+3.3V (out)	
78	Ground		77	Ground	
80	+1.8V (out)		79	+1.8V (out)	

2 J4 Pins 35,37,39,41 have alternate functionality NYI. When building an adapter board DO NOT CONNECT.

Connector pin notes:

- Port ID = Ground for VIN0. This is used to identify the port (VIN0(J3) or Vin1(J4)) to an external board attached to this port.
- Board ID pins (ID0, ID1, ID2, ID3) are used to identify the type of board attached to this connector. See Input Mezzanine Board Address section for details.
- Passthrough VIN and ground are passed through from main connector (J1) VIN and ground.
- See Video Input Port Description for details.

6.4 Connector J4: Video Input 1 (VIN1)

Connector: DF12(3.0)-80DP-0.5V(86) Mates with: DF12(3.0)-80DS-0.5V(86)

Similar pin-out as J3, except for the following:

PortID = +3.3V for Video Input 1, VINx = VIN1 for Video Input 1

Table 9: Video Input Pins

Pin	Description	Notes	Pin	Description	Notes
66	TX3	3.3V TTL	65	RX3	3.3V TTL
68	I2C3_SDA	/dev/i2c-4	67	I2C3_SCL	/dev/i2c-4
70	GP1_16_**ID1**	/sys/class/gpio/gpio48	69	GP0_20_**ID0**	sys/class/gpio/gpio20
72	GP1_18_**ID3**	/sys/class/gpio/gpio50	71	GP1_17_**ID2**	sys/class/gpio/gpio49
74	GP0_19	sys/class/gpio/gpio19	73	GP0_18	sys/class/gpio/gpio18

Connector pin notes:

- Port ID = +3.3 for VIN1. This is used to identify the port (VIN0(J3) or Vin1(J4)) to an external board attached to this port.
- Board ID pins (ID0, ID1, ID2, ID3) are used to identify the type of board attached to this connector. See Input Mezzanine Board Address section for details.
- Passthrough VIN and ground are passed through from main connector (J1) VIN and ground.
- See Video Input Port Description for details.

ⓘ SIGHTLINE USE ONLY

6.5 Connector J5: JTAG, JTAG, PIC Programmer

Connector: ZF5S-25-01-T-WT-TR

Test Points:

Label	Signal
TP1	Ground
TP2	Ground
TP3	Ground

7 Video Output Port Description

7.1.1 Signal Levels

Unless otherwise specified, all video signal levels are 3.3 Volts. See the table in Input Mezzanine Board Address for example video card accessories.

7.1.2 Power

There are multiple rails available on the connectors to power a mezzanine board or accessories. On the 3.3V rail, do not exceed 0.8A. On the 1.8V rail, do not exceed 0.7A.

7.2 Video Output

Vout (J2):

- Digital video output supporting up to 1080p60
- 20 Bit YCbCr (10Y/10CbCr) output, with lower 2 bits of Y and CbCr = 0
  - For 16-bit output, use upper 8 of Y and CbCr
  - YCbCr 4:2:2 format
- Currently only embedded sync has been validated (i.e., not using HSYNC/VSYNC/FLD/AVID)
  - Embedded Sync is BT1120 timing reference signals embedded in the data stream
- 3000-HDSDI-OUT board is a working design example of connecting an encoder to the J2 VOUT port
- Currently supported resolutions:
  - 720P60/59.94/50
  - 1080P60/59.94/50/30/29.97/25 (continued below)
  - 1080i60
  - 1080i59.94/50 (2.25 release)

Vout1 (alternate J3) (**not currently implemented**):

- 20-bit (10-bit Y, 10 CbCR) Digital video output
- Digital video output supporting up to 16-bit (YCbCr) / 24-bits (RGB)
- Other non-native formats such as 20-bit (10-bit Y, 10 CbCr) input may be possible with driver level development
- SD Composite / S-video (NTSC/PAL): ITU-R BT 470.6

HDMI Output (J1):

HDMI 1.3a (TBD 1.4a) compliant interface.

The HDMI output format is specified by the resolution and format specified through Panel Plus. The HDMI output ignores any EDID HDMI format information in the external HDMI sink device.

ⓘ **IMPORTANT:** Digital Video outputs (Vout, Vout1, HDMI) are incompatible with Analog video output on J1. Some combinations of Vout and HDMI can work simultaneously. Contact Support for more information.

8 Video Input Port Description

8.1 Overview

The 3000-OEM has 2x 16-bit video input ports - VIN0 / VIN1. Each input port can accept 1x 16-bit signal, or 2x 8-bit signals (Port A and Port B). The signals are parallel digital video only.

Two types of synchronization are supported. Both require a pixel clock along with the data stream:

- Discrete Video Sync Signals: Separates signals for Vertical Sync, Horizontal Sync, Field (interlace) and Data Valid.
- Embedded Sync: Synchronization codes present in the data stream are decoded to derive Vertical and Horizontal Sync and Field (interlaced) information. Data Valid is indicated by the presence of sync codes.
- Each input port only supports a single set of discrete video sync signals on Port A.
  - Only Embedded Sync video is supported when using 8-bit signals on Port B (BT.656).
  - All 8-bit input video (Port A or Port B) uses Embedded Sync.

The 3000-OEM supports interlaced video in Embedded Sync mode only (2.24 software release). Previous testing has indicated that the discrete field signal is inconsistently sampled by the hardware, resulting in swapping of field data over time.

8.2 Adapter boards

For acquiring video other than parallel digital video, a set of adapter boards are available to convert popular video signals to parallel digital video for input to the Video Ports. Details are available in ICD-3000-Adapter-Boards.

Input boards examples:

- Sony serial digital interface (Sony FCB cameras and compatible Tamron cameras)
- HD-SDI camera interface
- HDMI camera interface
- Camera Link camera interface
- Hitachi camera interface
- Analog Video (NTSC and PAL)
- Additionally, parallel video can be acquired using an adapter board that accepts an FFC and FPC cable types. Mating adapter boards are available that attach to specific camera types (Boson, Airborne, etc.)

SightLine adapter boards are often used by customers for system development work. The adapter board design is then integrated into a custom IO board that mates with the 3000-OEM.

8.3 Supported Standards

SMTPE 292 (Digital HD video):

- HD-SDI input adapter board
- Only 8-bits of Y and 8-bits of CrCb are acquired (use upper 8-bits if 10-bit data)
- Embedded sync signals are used to decode interlaced information. The DSP cannot reliably acquire field information from the VINx_FLD signal.

SMTPE 274 (analog HD video): TI TVP7002 analog to digital supported. Contact Support for details.

8.4 Signal Levels

Unless otherwise specified, all video signal levels are 3.3 Volts. See the table in Input Mezzanine Board Address for example video card accessories.

8.5 Power

There are multiple rails available on the connectors to power a mezzanine board or accessories. On the 3.3V rail do not exceed 0.8A. On the 1.8V rail, do not exceed 0.7A.

8.6 Video Formats

Vin0 (J3):

- 16-bit YCbCr (up to1920 x 1200 @ 60Hz)
- 16-bit grayscale (up to1920 x 1200 @ 60Hz)
- Embedded sync or external sync modes
- Dual clock independent 8-bit SD input. Port B supports embedded sync only

Vin1 (J4):

- 16-bit YCbCr (up to 1920 x 1200 @ 60Hz)
- 16-bit grayscale (up to1920 x 1200 @ 60Hz)
- Embedded sync or external sync modes
- Dual clock independent 8-bit SD input. Port B *(currently not functional)*

8.6.1 Camera Naming Convention

	When used as one 16-/24-bit input:	When used as two 8-bit inputs:
Connector	Appears in software as:	Appears in software as:
J3 (Vin0)	Camera 0 (Cam 0)	Camera 0 and Camera 1
J4 (Vin1)	Camera 2 (Cam 2)	Camera 2 and Camera 3*

* Not yet implemented

8.7 Color Camera Data Input Signal Locations

All signal locations refer to the table in Connector J3: Video Input 0.

16-bit YCbCr 4:2:2

- 8-bit luminance acquired in signal locations Y0->Y7
- 8-bit chrominance in signal locations CbCr0->CbCr7

20-bit YCbCr 4:2:2 (not supported)

Use upper 8-bits of 10-bit data for both Y and CbCr

8-bit BT.656

- Two camera inputs support port A and B of Vin0 / Vin1
- 8-bits in signal locations A0->A7 VIN0_ACLK (pixel clock)
- 8-bits in signal locations B0->B7 VIN0_BCLK (pixel clock). Port B not currently functional on VIN1.

Discrete Video Sync Signals in signal locations VINx_HSYNC, VINx_VSYNC, VINx_ACLK, VINx_FLD, VINx_DE (x= 0,1 for VIN0, VIN1)

Embedded Sync BT.1120, SMTPE296M/274M

8.8 Port Configuration and Compatibility

If port A is configured in 16 or 24-bit mode, port B is unavailable:

Port A	Port B
8-bit	OFF
16-bit	OFF
24-bit	OFF
8-bit	8-bit
OFF	8-bit

8.9 Grayscale Camera Data

Up to 16-bit (see Connector J3: Video Input 0)

8-bit data in signal locations G0 → G7 (G8 → G15 should be tied low)

14-bit data in signal locations G0 → G13 (G14 → G15 should be tied low)

16-bit data in signal locations G0 → G15

Discrete sync signals in signal locations VINx_HSYNC, VINx_VSYNC, VINx_ACLK, VINx_FLD, VINx_DE (where x is 0,1)

8.10 Synchronization Signals (Video Input 0 and 1)

The following synchronization signals are used. VINx refers to VIN0 or VIN1 depending on video input 0 or 1.

- VINx_VSYNC vertical sync: A rising edge (default) indicates the start of a new frame. This can be configured through acquisition parameters to falling edge.
- VINx_HSYNC horizontal sync: A rising edge (default) indicates the start of a new line. This can be configured through acquisition parameters to falling edge.
- VINx_ACLK pixel clock: Pixel data is sampled on the rising edge. Maximum input rate is 165 MHz. Clock edge is not currently configurable through acquisition parameters.
- VINx_FLD: This is the field signal for interlaced video. The 3000-OEM does not currently support interlaced acquisition using the field signal. However, starting in 2.24, the 3000-OEM will support interlaced video in embedded sync mode (still does not use VINx_FLD).
- VINx_DE: This is data enable or data valid. This signal is high only when active sensor pixel data is available. This signal will be low during vertical and horizontal blanking.

For detailed timing information, see TI document SPRS647e, section 8.10.1 HDVPSS Electrical Data/Timing.

8.11 Active Video Area and Blanking

Digital video signals contain blanking lines at the top of each frame known as vertical blanking. Blank pixels at the start of each line are known as horizontal blanking.

The active picture region is where the pixel data from the sensor is displayed (Figure 6). This example shows there are 45 blanking lines at the start of each frame, and 280 blanking pixels at the start of each row.

Every camera will have different vertical and horizontal blanking values. The same camera, when configured for different resolutions, can have different vertical and horizontal blanking values. Refer to the camera specific technical documentation for the correct settings.

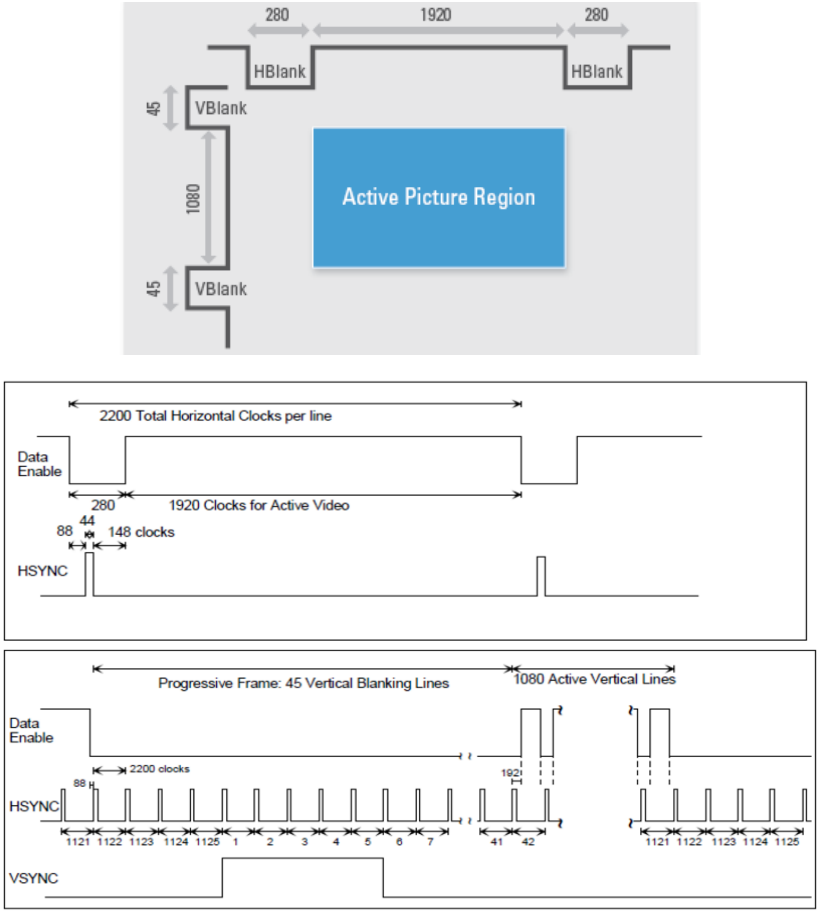

Figure 7: Vertical and Horizontal Blanking

8.11.1 Minimum Vertical Blanking Requirements

720P YCbCr video requires a minimum of 21 vertical blanking lines.

1080P YCbCr video requires a minimum of 30 vertical blanking lines.

ⓘ **IMPORTANT:** If the vertical blanking requirements are not met, the video may display the color artifacts along the top of the video as shown in Figure 7.

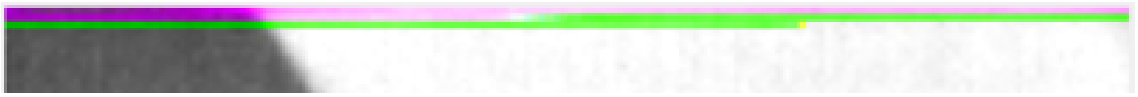

Figure 8: Color Artifacts in Video Example

Corrections:

Increase the vertical blanking of the camera output.

SightLine's default capture starts on rising edge of VSync. It is possible to start capture on the falling edge of VSync, which happens earlier, to get enough lines of blanking before active video starts. In Panel Plus, select the *Invert V-Sync Polarity* checkbox in *Acquisition Settings*. In the *Camera Type* drop down menu, select G*eneric Digital for the* camera type.

8.11.2 Removing Blanking Lines and Pixels

Blanking lines and pixels should automatically be removed when the video is acquired by the 3000-OEM.

There are two ways to set up automatic removal. In in the *Acquisition Settings* dialog window in Panel Plus, select the *Data Valid Signal* option in *Sync/Crop*, or if the Data Valid Signal is not supported, manually enter the *Vertical* and *Horizontal Front Porch* settings.

Data Valid Signal (if supported)

If the camera's data enable signal goes high when valid pixel data is available (active picture region), in the *Acquisition Settings* dialog, select *Data Valid Signal* in the *Syn/Crop* dropdown menu. Leave *Vertical Front Porch* and *Horizontal Front Porch* set to 0. The 3000-OEM hardware will use the data valid signal to remove blanking lines and pixels from the acquired video.

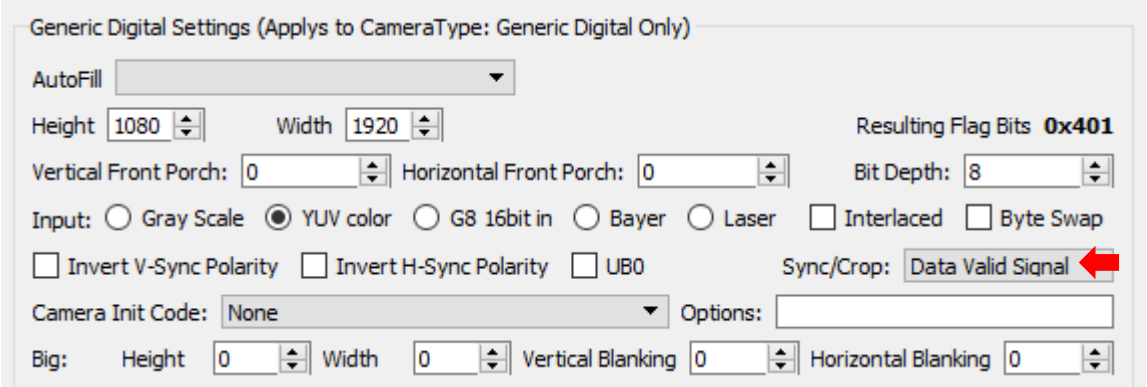

Figure 9: Data Valid Supported

Vertical and Horizontal Front Porch (manual blanking entry)

If the camera does not support Data Valid Signal setting, set the *Sync/Crop* to *None*. Set the *Vertical Front Porch* (blanking) to *45*. Set *Horizontal Front Porch* (blanking) to *280*.

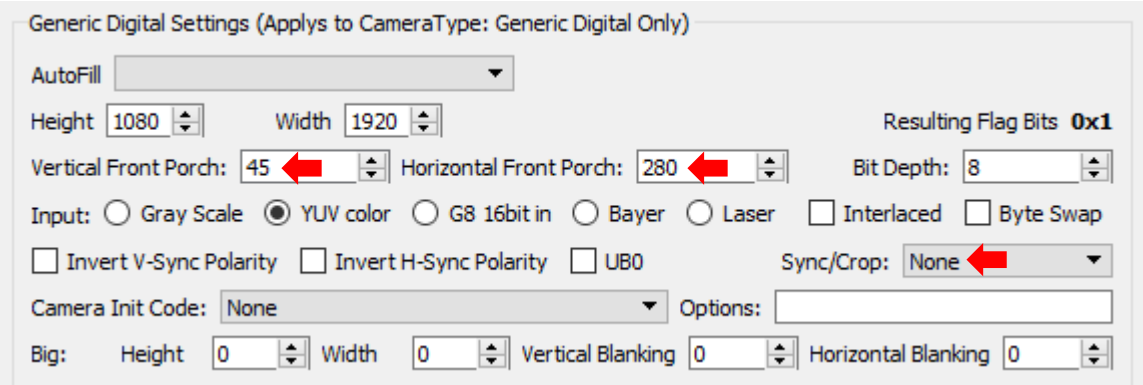

Figure 10: Data Valid Not Supported

If using a custom camera, or a technical reference manual that shows the vertical and horizontal blanking is not available:

1. Set *Vertical Front Porch* and *Horizontal Front Porch* to *0*.
2. Turn off stabilization (Panel Plus main menu *» Configure » Stabilization » Disable All Processing*).
3. Disable *AutoChop* for the camera (Panel Plus main menu » *Configure » Margin Chopping*).
4. Save the parameters to the board, and then reboot the system. The network video should be viewable in Panel Plus.
5. Point the camera at a bright white scene. Rows at the top or columns at the left that remain gray are blanking areas.
6. Performa an SD card snapshot with Capture as the source. See EAN-File Recording.
7. Download the snapshot and open it in an image viewer application. Zoom in and count the number of blank lines at the top (vertical blanking) and blank columns at the left (horizontal blanking).
8. If an SD Card snapshot cannot be taken, change the horizontal and vertical blanking values. Save the parameters to the board, and then restart the board. View the video in Panel Plus and repeat until all the blanking lines have been removed.

9 Input Mezzanine Board Address

Each of SightLine's camera adapter boards is assigned a unique adapter ID to simplify setup and configuration. This applies to any board connected to J3 or J4. Use 10k Ohm resistors to pull up (bit value 1) or pull down (bit value 0) to set the address.

In the future, camera configuration will be overwritten in software using SightLine's Command and Control Protocol. If designing a custom camera board to connect to the 3000-OEM, contact SightLine Applications to discuss the correct board address to use.

Table 10: 3000-OEM Mezzanine Board ID Table

Board ID	72	71	70	69	Board Description	Part Number
0x0	0	0	0	0	No board	(Default) No board connected. No video acquired.
0x1	0	0	0	1	Sony block adapter	SLA-3000-Sony
0x2	0	0	1	0	Camera Link® adapter	SLA-3000-CL
0x3	0	0	1	1	Analog video adapter	SLA-3000-AB (Dual Analog)
0x4	0	1	0	0	HDSDI adapter	SLA-3000-HDSDI Input
0x5	0	1	0	1	Hitachi adapter	SLA-3000-HITACHI
0x6	0	1	1	0	FFC/FPC adapter	SLA-3000-FFC, SLA-3000-FPC
0x7	0	1	1	1	HDMI camera	SLA-3000-HDMI
0x8 – 0xC	-	-	-	-	Reserved	
0xD	1	1	0	1	Generic adapter	Generic adapter board *
0xE	1	1	1	0	Special custom board	Do not use
0xF	1	1	1	1	*Reserved for future use*	

***** *For Generic Adapter ID (0xD) the GPIO pins must be pulled to 0xD by the adapter board. For customer designed adapter boards that copy the SLA adapter board schematics, make sure any decoder or other adapter hardware is enabled with the GPIO pins at 0xD. It is common for SLA designed adapter boards to repurpose these GPIO pins once the board ID is read. The same cannot be assumed for generic adapter boards.*

10 Questions and Additional Support

For questions and additional support, please contact Technical Support. Additional support documentation and Engineering Application Notes (EANs) can be found on the Support pages of the SightLine Applications website.