



ICD-1500-OEM

2021-12-22

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1	Overview	1	6.1	OEM Power	8
1.1	Additional Support Documentation	1	6.2	Camera Power Considerations.....	8
1.2	Sightline Software Requirements	1	6.3	VIOSEL - Setting IO Signal Levels	9
2	Safe Device Handling.....	1	6.4	LEDS	9
3	1500-OEM Overview	1	6.5	Serial Ports	9
3.1	1500-OEM Specifications	2	6.6	Test Points.....	10
3.2	Hardware Revisions.....	2	6.7	GPIO	10
3.3	Interface Protocol	2	7	Digital Video Input Description	11
3.4	Primary Input / Output	2	7.1	Overview.....	11
3.5	Functional Block Diagram	3	7.2	Adapter boards	11
3.6	1500-SOM	3	7.3	Signal Levels.....	11
3.6.1	Design Support.....	3	7.4	Synchronization Signals	12
4	Thermal Management	3	7.5	Video Formats.....	12
4.1	Heatsink Guidelines	3	7.6	Color Camera Data Input Signal Locations.....	13
4.2	Gap Filler (Thermal Grease)	4	7.7	Grayscale Camera Data.....	13
4.3	Gap Pads	4	7.8	Active Video Area and Blanking	13
5	Connector Summary	4	7.8.1	Removing Blanking Lines and Pixels	14
5.1	Connector J3	4	8	Questions and Additional Support.....	14
5.1.1	Analog Video Input.....	5	Appendix A - Missing Driver Chip	15	
5.1.2	Analog Video Out	5	Appendix B - Anti-Alias Filter	15	
5.1.3	Ethernet	5	Appendix C - Analog Input Noise Shielding.....	16	
5.2	Connector J4	6	Appendix D - Level Translators	17	
5.2.1	Internal Pullup on J4 Pins.....	7	D1	Overview	17
5.3	Connector J5: FPGA JTAG, USB, GPIO	7	D2	Recommended Level Translators.....	17
5.4	Socket S1: MicroSD	7	D3	Level Translation Overview.....	17
6	Additional I/O.....	8	D4	Example: Driving a BOB-12009 with TXB0104	18

 **CAUTION:** Alerts to a potential hazard that may result in personal injury, or an unsafe practice that causes damage to the equipment if not avoided

 **IMPORTANT:** Identifies crucial information that is important to setup and configuration procedures.

 *Used to emphasize points or reminds the user of something. Supplementary information that aids in the use or understanding of the equipment or subject that is not critical to system use.*



Revision History

Date	Description
2021-09-01	Added Appendix D - Level Translators. Filled in software signal names in GPIO table.
2020-02-11	Added serial port and GPIO tables in I/O section. Added camera power guidance sections.
2020-09-18	Added note that the USB communications interface is not available on connector J5.
2020-09-14	Add I2c bus speed (400 kHz) to Primary Input / Output section.
2020-01-08	Add section on Digital Video Input Signal.
2020-01-02	Corrected the processor P/N (DM8148 to DM3730) in the Interface Protocol section.
2019-10-17	Added voltage qualification note to specifications.
2019-03-22	Added Caution statement on board modifications.
2018-12-12	Updated Thermal Management section with temperature related commands in the IDD.
2018-09-10	Added voltage and power to spec table. Added supply voltage level compatibility statement for camera boards.
2018-08-01	Added caution statement in the Connector section for powering up specific types of interface boards.
2018-07-26	Added Appendix C - Analog Input Noise Shielding
2018-06-12	Added Ethernet magnetics information.
2018-03-16	Added default direction and values of GPIO pins.
2018-03-06	Minor updates to VIOSEL.
2018-02-27	Updated SOM section.
2017-12-20	Updated Thermal Management section.
2017-12-05	Updated document to new format. Created new ICD document for 1500-OEM adapter boards.
2017-10-05	Split document into ICD-1500-OEM and ICD-1500-ADAPTERS. Minor diagrams, text, and tables syntax edits.
2017-08-24	Cross reference power definitions, added clarification to serial port # and pin names as well a cross references for easy lookup.
2017-07-18	Updated power input requirements.
2017-04-12	Fixed J4 pinout. Added more details regarding the serial port.
2016-08-15	Schematics moved to separate files, added Rev E information.
2015-10-19	Added 1500-mAB section.
2015-09-17	Updated 1500-AB connectors, added 1500-Sony table captions, added illustrations for 1500-Sony J3 Pin 1.
2015-09-15	Updated hardware overview, added IO block diagram, added accessories summary section, updated connector details for 1500-Sony, corrected copyright.
2015-05-11	Formatting, minor text and table edits, fix 1500-AB J3 table, Copyright dates, added Revision History, Figures and Table indexes.



1 Overview

Describes power requirements, thermal management, interface specifications, and connector pinouts for the 1500-OEM video processing board.

CAUTION: Any customer modifications to SightLine OEM and adapter boards will void the warranty and can potentially damage the board. Before attempting any modifications, please contact [Support](#).

1.1 Additional Support Documentation

Additional Engineering Application Notes (EANs) can be found on the [Documentation](#) page of the SightLine Applications website.

The [Panel Plus User Guide](#) provides a complete overview of settings and dialog windows located in the Help menu of the Panel Plus application.

The Interface Command and Control ([IDD](#)) describes the native communications protocol used by the SightLine Applications product line. The IDD is also available as a PDF download on the [Documentation](#) page under Software Support Documentation.

1.2 Sightline Software Requirements

IMPORTANT: The Panel Plus software version should match the firmware version running on the board. Firmware and Panel Plus software versions are available on the [Software Download](#) page.

2 Safe Device Handling

CAUTION: To prevent damage to hardware boards, use a conductive wrist strap attached to a good earth ground. Before picking up an ESD sensitive electronic component, discharge built up static by touching a grounded bare metal surface or approved antistatic mat.

3 1500-OEM Overview

The 1500-OEM from SightLine Applications is a small, low power, single-channel on-board video processor for unmanned airborne or ground vehicles in ISR applications.

The system is capable of processing and streaming HD video outputs up to 720P. This product is designed to add advanced capabilities to camera systems. It operates on video right at the source, which is key for low latency performance and best video quality.

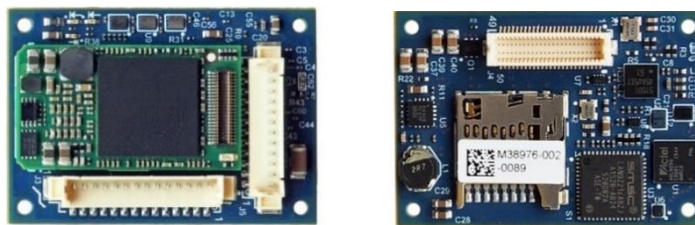


Figure 1: 1500-OEM Overview



3.1 1500-OEM Specifications

Revision:	E
Dimensions:	1.48 in x 1.04 in (26.5 mm x 37.7 mm)
Weight:	7.6 grams
Voltage:	4.5 - 6 VDC OEM (5V nom) ¹
Power:	3 W (max) 2.5W (typical)
Drawing:	1500-OEM Drawings*
STEP File:	1500-OEM STEP Files*

*Includes all production release revisions.

All mounting holes support M1.6 screws.

ⓘ IMPORTANT: The supply voltage level must be compatible with the camera adapter board and connected cameras.

3.2 Hardware Revisions

Board Revision	Changes
Rev E	<ul style="list-style-type: none"> Added 2 GPIO ports on (J5) - GPIO 144 and GPIO 145. Onboard FPGA programming no longer requires external JTAG emulator hardware. Improved boot-time by three seconds. Replaced microSD card with smaller version. Added fourth mounting hole. Fixed USB hardware (J5)*.
Rev C	Initial production release.

* The USB communications interface is not currently available. Use of this feature is contingent on software updates.

3.3 Interface Protocol

The 1500-OEM shares the same interface protocol as other SightLine OEM platforms. The protocol is a packet-based command and control interface (IDD). The protocol document is also available as a PDF from the SightLine [website](#).

The ARM core on the DM3730 is only lightly utilized during implementation. This provides customers with a processor to implement other processing functions or protocol conversions, i.e., allows communications through customized proprietary protocols.

3.4 Primary Input / Output

- 4.5 - 6.0 VDC (5 VDC nominal)¹
- Analog Video In (x2)
- 10/100Base-T Ethernet
- 7 GPIO
- USB 2.0 (contingent on software updates)
- Digital Video Input (16-bits + clocks)
- TTL Serial Ports (x3)
- I2C (3.3V, 400 kHz)
- On-board FPGA for advanced video signal processing
- MicroSD Card

¹ A slightly extended input voltage range is possible with some tradeoffs. Contact [Support](#) for more information if this is relevant to your application.



3.5 Functional Block Diagram

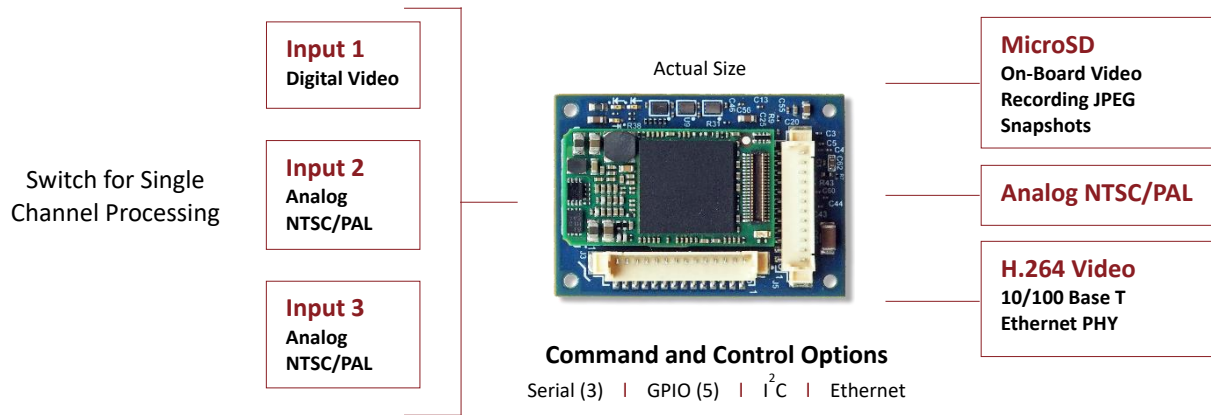


Figure 2: 1500-OEM Functional Block Diagram

3.6 1500-SOM

The SOM hardware is a small profile (15 x 27 mm) and low power (2.25W) Beacon EmbeddedWorks Torpedo 3730 System-on-Module (p/n: SOMDM3730-20-1780AGIR).

IMPORTANT: Do not remove the 1500-SOM from the 1500-OEM board.

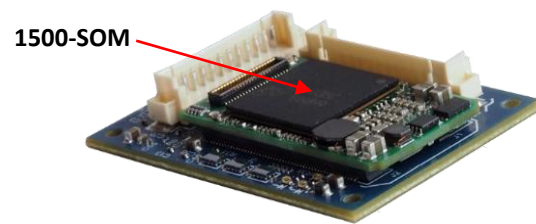


Figure 3: 1500-SOM Orientation

3.6.1 Design Support

SightLine actively supports customer development of new interface circuit boards that will optimize integration of our video processors into production designs. The 1500-SOM is the smallest form factor option to incorporate SightLine video processing functions into customer designs. Access to reference design files for 1500-SOM carrier board (1500-OEM board) is provided under the terms of a simple Hardware Design IP Agreement document. Contact [Sales](#) for more information.

4 Thermal Management

4.1 Heatsink Guidelines

- Component temp range: -40°C to 85°C
- All hardware uses some form of mechanical heatsink.
- The 1500-OEM consumes approximately 2.5 watts of power. Most of the power used is by the DSP + memory PoP (Part-on-Part) on the SOM.
- The blue stick-on heatsink included in the EVAL Kit facilitates bench testing. It can also be purchased separately from Advanced Thermal Solutions (PN: ATS-52150P-C1-R0) or SightLine (PN: SLA-1500-HSNK). It supports convective cooling when there is airflow.



- ❗ **IMPORTANT:** The blue stick-on heatsink is not intended for long term vehicle integration use. A more robust solution should be designed and implemented by the integrator.
- When designing a custom heatsink for integration, it should provide a direct conducted path to a significant thermal mass (typically the wall of a gimbal or housing).
- If there is enough airflow, multiple finned options are available including thermal epoxy for mounting. Fin design should be selected based on airflow and available space.
- ❗ **IMPORTANT:** The 1500-OEM does not have an automatic thermal processor shutdown. The operating temperature of the unit can be read through the **SLAGetVersionNumber (0x00)** command. The temperature can also be reported continually using the **System Status Message (0x87)** command. See the [IDD](#) for more information.

4.2 Gap Filler (Thermal Grease)

When possible, use some form of thermally conductive liquid gap filling material such as [Arctic Silver](#) rather than an adhesive. Do not use thermal grease in conjunction with gap pads.

4.3 Gap Pads

Use some form of thermally conductive material for filling gaps between the hot components and the heat sink. Examples such as the [Bergquist](#) VO Ultra Soft are recommended. Do not use gap pads in conjunction with thermal grease.

5 Connector Summary

Table 1: Connector Summary

Label	MFG Part Number	Function	Mates with:
J3	Molex 53398-1471	Analog video in/out, power, serial, Ethernet	Molex 51021-1400
J4	Hirose DF12B(5.0) 50DP-0.5V(86)	Serial, digital video, I2C, etc.	Hirose DF12B-50DS-0.5V(86)
J5	Molex 53398-1271	FPGA JTAG, USB (coming soon), GPIO	Molex 51021-1200
S1	JEA ST9S008V4AR1500	J Micro SD socket	Any Micro SD card

5.1 Connector J3

Analog Video, Power, Serial 0, Ethernet

Table 2: 1500-OEM J3 Pinout

Pin	Signal	Description	Pin	Signal	Description
1	Video In 0	Analog video input	8	Vin	Input 4.5 - 6.0 VDC
2	AGND		9	Vin	
3	Video Out	Analog video output	10	DGND	10/100BaseT Ethernet
4	AGND		11	RX-	
5	TX0	Serial port 0	12	RX+	
6	RX0		13	TX+	
07	DGND		14	TX-	

⚠ **CAUTION:** On some interfaces, e.g., 1500-Sony / Tamron board, power to the 1500-OEM board is provided through J4 on pins 48 and 50. In these cases do not apply power to J3 pins 8 and 9. Powering the OEM through the J3 power pins and through the J4 power pins can damage the OEM.



5.1.1 Analog Video Input

Supports the following analog video formats:

- NTSC-J, M
- PAL-B, D, G, H, I
- PAL-M
- Converts luminance and chrominance channels to 8-bit ITU-R BT.656 interface with embedded sync output and extended coding range of values.
- Y, U, and V range from 1 to 254.

ⓘ IMPORTANT: See [Appendix C](#) for more information on minimizing noise on analog input.

5.1.2 Analog Video Out

Composite TV out.

Supports composite DC coupled full-scale voltage output: minimum 1.2 V_{pp} with a 75-Ω parallel termination. The following video standards are supported:

- NTSC-J, M
- PAL-B, D, G, H, I
- PAL-M

A 75Ω parallel resistor (to ground) is required on the TV-out for proper signal quality. Video traces should be routed with 75Ω characteristic impedance.

5.1.3 Ethernet

On connector J3, pin 11 through pin 14 represent the Ethernet connection. Currently only 10/100BASE-T has been implemented.

TX+/ TX- is sending info from Sightline product., RX+/ RX- is receiving.

The 1500-OEM uses the embedded Ethernet approach. This consists of 0.033uF capacitors placed in series on the Ethernet lines (AC coupled) onboard. There are no Ethernet magnetics on the 1500-OEM. If the distance is less than a few meters and there is a common ground, there should not be any issues with Ethernet connectivity (even in EMI testing).

ⓘ IMPORTANT: If the Ethernet needs to be changed to use external magnetics, the OEM board should be modified by changing the board capacitors (and possibly other passives) to zero Ω jumpers. Contact [Support](#) for modification assistance.



5.2 Connector J4

Digital Camera, Serial Ports, GPIO, Alternate Input Power.

This connector is designed to allow the 1500-OEM to mate with the FLIR Tau 640 or other SightLine system interface boards. This is a generic camera input supporting up to 12-bits video data. The 1500-SOM can accept many types of digital video input. For optimal processing performance, the height and width of the image should be a multiple of 16.

CAUTION: On some interfaces, e.g., 1500-Sony / Tamron board, power to the 1500-OEM board is provided through J4 on pins 48 and 50. In these cases do not apply power to J3 pins 8 and 9. Powering the OEM through the J3 power pins and through the J4 power pins can damage the OEM.

Table 3: 1500-OEM J4 Pinout

Power		Analog Video		Digital Video		12C		Serial		GPIO		Ground	
Pin	Description	Signal Level	Pin	Description	Signal Level								
1	RX2	VIOSEL	2	TX2	VIOSEL								
3	CAMD14 / CAMXCLKA	VIOSEL	4	CAMD15 / CAMXCLKB	VIOSEL								
5	DGND		6	DGND									
7	I2C SCL	VIOSEL	8	I2C SDA	VIOSEL								
9	GPIO175	VIOSEL	10	CAMFLD	VIOSEL								
11	CAMVS	VIOSEL	12	CAMHS	VIOSEL								
13	GPIO174	VIOSEL	14	GPIO173	VIOSEL								
15	RX1	VIOSEL	16	TX1	VIOSEL								
17	DGND		18	TAUDET									
19	GPIO178	3.3V	20	CAMD13	VIOSEL								
21	EXTSYNC (Future Use)	VIOSEL	22	CAMD12	VIOSEL								
23	CAMD11	VIOSEL	24	CAMD10	VIOSEL								
25	CAMD09	VIOSEL	26	CAMD08	VIOSEL								
27	DGND		28	DGND									
29	CAMD07	VIOSEL	30	CAMD06	VIOSEL								
31	CAMD05	VIOSEL	32	CAMD04	VIOSEL								
33	CAMD03	VIOSEL	34	CAMD02	VIOSEL								
35	CAMD01	VIOSEL	36	CAMD00	VIOSEL								
37	DGND		38	DGND									
39	CAMPCLK	VIOSEL	40	GPIO172	VIOSEL								
41	DGND		42	DGND									
43	Analog Video In 1		44	Analog Ground									
45	DGND		46	VIOSEL	See VIOSEL - Setting IO Signal Levels								
47	Power Return		48	Alternate Power In/Out	5V								
49	Power Return		50	Alternate Power In/Out	5V								



5.2.1 Internal Pullup on J4 Pins

The pullup drive strength is equal to: minimum = 50 μ A, typical = 100 μ A, maximum = 250 μ A (unless otherwise specified).

See [Appendix D - Level Translators](#) for more information.

5.3 Connector J5: FPGA JTAG, USB, GPIO

Connector J5 is rarely used in system implementations and is typically not connected to.

The USB_VBUS connection can supply a maximum of 100mA. If using as a power source for connected devices that require more than 100mA, they will need an external power source.

Use of JTAG pins to program the input FPGA is not needed for the Rev E. See [EAN-FPGA-Firmware-Update-1500-OEM](#).

IMPORTANT: The USB communications interface is not currently supported. This content may change as more information becomes available. For any additional questions contact [Support](#).

Table 4: 1500-OEM (Rev E) J5 Pinout

Pin	Description	Pin	Description
1	USB_VBUS	7	FPGA JTAG TMS
2	USB-	8	FPGA JTAG TDI
3	USB+	9	GPIO145
4	USBID	10	FPGA JTAG TRST
5	DGND	11	FPGA JTAG TDO
6	FPGA JTAG TCK	12	GPIO144

5.4 Socket S1: MicroSD

Push the microSD into place. To eject push it again. The socket is rated up to 10,000 mating cycles and has 3.3 mm card eject length.

Recommended MicroSD card types and previously tested models are discussed in the [EAN-File-Recording](#) document.

On Rev E boards use an adhesive to hold the microSD card in place to prevent ejection during hard aircraft landings or other shocks to the board.

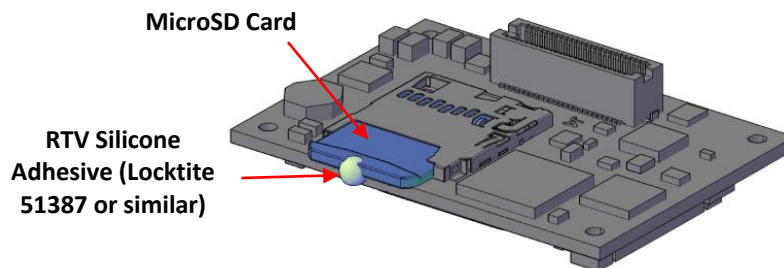


Figure 4: Example - 1500-OEM (Rev E) Adhesive Placement on MicroSD Card



6 Additional I/O

6.1 OEM Power

OEM power can be applied to either J3 or J4.

Table 5: 1500-OEM Power Supply Pins

Connector/Pin	Name	Range	Notes
J3 Pin 8 and 9	P5V	4.5 - 5.5V	Primary (typical) power input pins
J4 Pin 48 and 50	P5V	4.5 - 5.5V	Alternate power input if powering via the digital interface connector (ex: Sony Input Adapter or customer interface)

ⓘ IMPORTANT: Do not apply power to both J3 and J4 pins at the same time. On some interfaces, e.g., 1500-Sony / Tamron board, power to the 1500-OEM board is provided through J4. In these cases, do not apply power to J3. Powering the OEM through the J3 power pins and through the J4 power pins can damage the OEM.

6.2 Camera Power Considerations

Integrators should understand how camera power is provided and how it impacts use of the 1500-OEM. There are three camera power categories for the 1500-OEM camera interfaces:

- Cameras powered from the OEM.
- Camera configurations that provide power to the OEM.
- Camera power independent of SightLine circuits.

Table 6: Cameras Powered from 1500-OEM

Camera	Camera Interface Adapter	Notes / Warnings
FLIR Tau	SLA-1500-FFC	VIN directly to camera. Be aware when setting OEM input voltage. Current provided to camera is limited only by connector pin current ratings.
DRS Tamarisk	SLA-1500-FPC	
HDMI	SLA-1500-HDMI	
Airborne Innovations	SLA-1500-FPC	⚠ CAUTION: The camera input voltage for this camera is less than max VIN to OEM. Ensure the OEM VIN is set correctly to avoid camera damage.
FLIR Boson 320	SLA-1500-FPC	Limited to (810mA) of camera power. This meets camera specifications for the Boson 320 camera, but slightly below max power required for the Boson 640 camera. Even though tests have shown that OEM power to the Boson 640 is adequate, SightLine recommends using external power for the camera - see Table 8 below.

Table 7: Camera Configurations Providing Power to 1500-OEM

Camera	Camera Interface Adapter	Notes
Hitachi Block	SLA-1500-HIT	Camera adapter board has 5V regulator to power OEM. External power applied to adapter should meet camera voltage requirements
Sony, Tamron, Intertest and other Sony type block cameras.	SLA-1500-SONY	

ⓘ IMPORTANT: Do not apply power to J3 when using these configurations. Power to the OEM is provided on J4.

**Table 8: Cameras Powered Independently**

Camera	Camera Interface Adapter	Notes
Camera Link	SLA-1500-CL	SightLine Adapter Boards do not provide options for providing power to the camera. Follow guidance from camera manufacturers
Analog	OEM input on J3 / J4	
FLIR Boson 640 FPC-Boson Ext Option	SLA-1500-FPC	The FPC-Boson-EXT board provides the ability for customers to provide external power to the camera. The 1500 OEM can only provide (810mA) of power through the interface, which is below the max input current specification of the Boson 640 camera.
Other	NA	Other cameras that provide power support through independent input connectors unassociated with SightLine connections

- ⓘ IMPORTANT:** The supply voltage level must be compatible with camera adapter board and connected cameras. For example, the 3000-Sony camera adapter board passes supply voltage directly to the attached camera. A Sony EH series camera can only support 6V - 12V. This would limit the supply voltage to the 4000-OEM to this range.
- ⓘ IMPORTANT:** There are multiple rails available on the connectors to power a camera adapter board or accessories. Do not exceed 0.8A on the 3.3V rail. Do not exceed 0.7A on the 1.8V rail.

6.3 VIOSEL - Setting IO Signal Levels

Pin 46 VIOSEL powers and sets the voltage level of the signals with names starting with CAM, as well as the GPIOs, RX1/TX1 and RX2/TX2. VIOSEL can be set to 1.8V, 2.5V, or 3.3V. All signals besides the CAM signals use the bidirectional level converter TXB0108, which has a weak steady state drive strength.

- ⓘ IMPORTANT:** Do not exceed 3.3V on VIOSEL.

6.4 LEDS

Table 9: 1500-OEM LED Status

Label	Description	LED Color
D1	Power Indicator	Green
D2	GPIO179	Green
D3	Network Status	Green

6.5 Serial Ports

To use serial port 1 and serial port 2, external power must be applied to VIOSEL to set the IO voltage level.

Serial port 0 operates at 3.3V. If an application requires a different IO voltage for serial port 0, it is important to use a level shifter that is not a bidirectional, i.e., an automatic direction sensing type of level shifter.



Table 10: Serial Port Summary

Ports	Serial 0	Serial 1	Serial 2	Notes
Linux Reference	/dev/ttyO0	/dev/ttyO1	/dev/ttyO2	Useful for command line testing, or custom ARM applications.
SOM Port Number	A	C	B	The Torpedo SOM hardware uses a different nomenclature in the documentation. The SOM serial port (A, B, C) maps to the SLA serial port (0, 2, 1).
Used for:	Command and Control and debug. Recommend maintaining access for troubleshooting.	Command and Control and general customer use/passthrough.	Primarily camera control passthrough, can be used for general customer use/passthrough or command and control.	

Table 11: Serial Ports - 1500-OEM

Serial Ports	Serial 0			Serial 1			Serial 2			Notes
	Connector, Pin			Connector, Pin			Connector, Pin			
1500-OEM	Rx	Tx	Level	Rx	Tx	Level	Rx	Tx	Level	Voltage levels of serial 1 and 2 are set by VIOSEL input J4,46.
	J3,6	J3,5	3.3V	J4,15	J4,16	Note	J4,1	J4,2	Note	

ⓘ IMPORTANT: It is not necessary to apply power to VIOSEL when using a SightLine accessory board other than 1500-AB development board that implements serial 1 and/or serial 2. These boards have a DC-to-DC converter that provides 3.3V to VIOSEL. Powering VIOSEL through both the internal regulator and an external source can have unpredictable results and potentially damage the OEM and accessory boards.

Serial port mapping when using system and camera interface boards are defined in the ICD-1500-Adapter-Boards document.

6.6 Test Points

Table 12: 1500-OEM Test Points

Label	Description	Label	Description
TP1	Ground	TP3	FPGA Pin B9
TP2	3.3V	TP4	FPGA Pin C8

6.7 GPIO

See the [ICD-1500-Adapter-Boards](#) for GPIO mapping when using system and camera interface boards.

Table 13: 1500-OEM GPIO

Hardware Reference	Pin	Level	Pin	Level	Pin	Level	Pin	Level	Pin	Level	Pin	Level	Pin	Level (3.3V)	Notes
OEM Schematic Reference	GPIO144		GPIO145		GPIO172		GPIO173		GPIO174		GPIO175		GPIO178		
SW Signal Name	/sys/class/gpio/gpio144		/sys/class/gpio/gpio145		/sys/class/gpio/gpio172		/sys/class/gpio/gpio173		/sys/class/gpio/gpio174		/sys/class/gpio/gpio175		/sys/class/gpio/gpio178		
1500-OEM	J5,12	1.8V	J5,9	1.8V	J4,40	Note	J4,14	Note	J4,13	Note	J4,9	Note	J4,19	3.3V	Voltage levels of four of the J4 GPIO signals are set by VIOSEL input J4,46.
Default State	Input		Input		Output		Input		Input		Input		Input		
Default Value	Low		Low		Low		High		High (may toggle on startup)		High		Low		Default value may change based on SW release. Contact SightLine if this is important.



Table 14: 1500-OEM GPIO Signals Not Accessible

Schematic Signal Name	Software Signal Name	Reference Voltage	Description/Location
GPIO129	NA	1.8V	LAN9221 Pin 43
GPIO171	/sys/class/gpio/gpio171	1.8V	FPGA A9
GPIO179	/sys/class/led/led2	3.3V	LED D2 (green) - Used to indicate firmware update progress.

7 Digital Video Input Description

7.1 Overview

The 1500-OEM has a single 16-bit digital video input port - Cam 2 (Digital). The signals are parallel digital video only. (Also referred to as *CMOS video*.)

Signal locations are detailed in [Table 3: 1500-OEM J4 Pinout](#).

Two types of synchronization are supported. Both require a pixel clock along with the data stream:

- Discrete Video Sync Signals: Separate signals for vertical sync and horizontal sync
- Embedded Sync: Synchronization codes present in the data stream are decoded to derive vertical and horizontal sync and field (interlaced) information. This requires using FPGA V7 for BT.1120 (HD) embedded sync. BT.656 embedded sync (SD) is supported natively in the 1500 DSP.
- Details on signals and pin locations are in section [Video Formats](#).

7.2 Adapter boards

For acquiring video other than parallel digital video, a set of adapter boards are available to convert popular video signals to parallel digital video for input to the Video Port. Details are available in [ICD-1500-Adapter-Boards](#).

Input boards:

- Sony serial digital interface (Sony FCB cameras and compatible Tamron cameras)
 - HDMI camera interface
 - Camera Link camera interface
 - Hitachi camera interface
 - Additionally, parallel video can be acquired using an adapter board that accepts an FFC and FPC cable types. Mating adapter boards are available that attach to specific camera types (Boson, Airborne, etc.)
- i** *SightLine adapter boards are often used by customers for system development work. The adapter board design is then integrated into a custom IO board that mates with the 1500-OEM.*

7.3 Signal Levels

Unless otherwise specified, all video signal levels are at the voltage provided by the VIOSEL reference level input to the 1500-OEM. See the [VIOSEL - Setting IO Signal Levels](#) section.



7.4 Synchronization Signals

The following synchronization signals are used. See [Table 3: 1500-OEM J4 Pinout](#).

- CAMVS vertical sync: A rising edge (default) indicates the start of a new frame.
 - CAMHS horizontal sync: A rising edge (default) indicates the start of a new line.
 - CAMFLD: This is the field signal for interlaced video. The 1500-OEM does not currently support interlaced acquisition using the field signal.
 - CAMPCLK pixel clock: Pixel data is sampled on the rising edge. Maximum input rate is 74.25 MHz. Pixel clock edge is not currently configurable through acquisition parameters.
- i IMPORTANT:** For 16/14-bit digital parallel video inputs, in most cases the customer is required to externally double the pixel clock that is provided to the 1500-OEM. For 720P60 or 1080P30 cameras in this case, the input pixel clock to the 1500-OEM CAMPCLK will be externally doubled to 148.5 MHz. This does not apply to camera data provided through Sightline adapter boards since these boards implement this pixel clock doubling where necessary. Contact [Sightline Support](#) for details.

7.5 Video Formats

Video synchronization can be accomplished using either Discrete Sync signals or Embedded Sync data. Generally Discrete Signals are preferred as they are more commonly supported in the 1500-OEM.

Discrete Video Sync Signals in signal locations

- CAMVS (Vertical sync, start of frame)
- CAMHS (Horizontal sync, start of line)
- CAMFLD (field) – not generally used.

Embedded Sync In this case all synchronization information is in the embedded sync codes - only the pixel clock and the data stream are used.

- BT.1120 (HD, 720/1080P 30 FPS) Requires special FPGA version 7, only process 720P
- BT.656. (SD – 525/625 lines)

Cam 2 (Digital) (J4):

- 16-bit YCbCr (up to 1920 x 1080 @ 30Hz) – 1500-OEM only processes center 720P
- 16-bit grayscale (up to 640x512 @ 30Hz)
- Embedded sync or discrete sync modes



7.6 Color Camera Data Input Signal Locations

All signal locations refer to the [Table 3: 1500-OEM J4 Pinout](#).

16-bit YCbCr 4:2:2

8-bit luminance Y acquired in signal locations CAMD08->CAMD15

8-bit chrominance CbCr in signal locations CAMD00->CAMD07

8-bit BT.656

8-bits BT.656: Data on signal pins CAMD00->CAMD07

7.7 Grayscale Camera Data

Up to 16-bit

8-bit data in signal locations CAMD00->CAMD07 (CAMD08->CAMD15 should be tied low)

14-bit data in signal locations CAMD00->CAMD13 (CAMD14->CAMD15 should be tied low)

16-bit data in signal locations CAMD00->CAMD15

Discrete sync signals in signal locations CAMVS, CAMHS

7.8 Active Video Area and Blanking

Digital video signals contain blanking lines at the top of each frame known as vertical blanking. Blank pixels at the start of each line are known as horizontal blanking.

The active picture region is where the pixel data from the sensor is displayed ([Figure 5](#)). This example shows there are 45 blanking lines at the start of each frame, and 280 blanking pixels at the start of each row.

Every camera will have different vertical and horizontal blanking values. The same camera, when configured for different resolutions, can have different vertical and horizontal blanking values. Refer to the camera specific technical documentation for the correct settings.

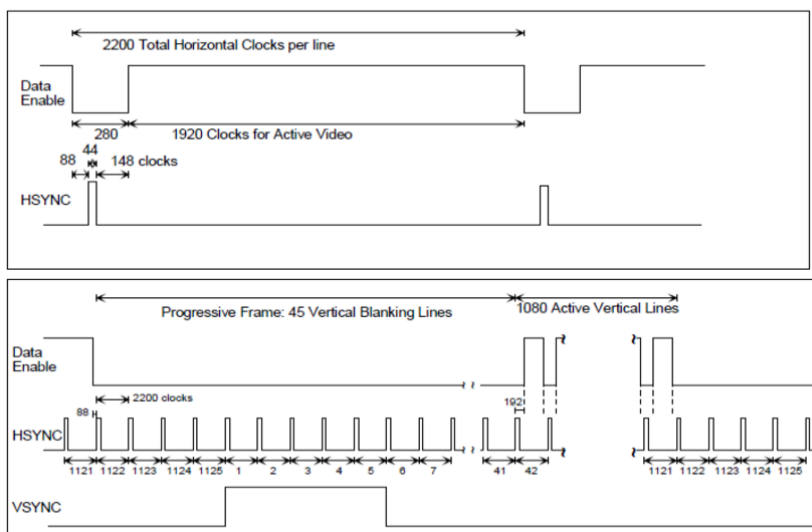
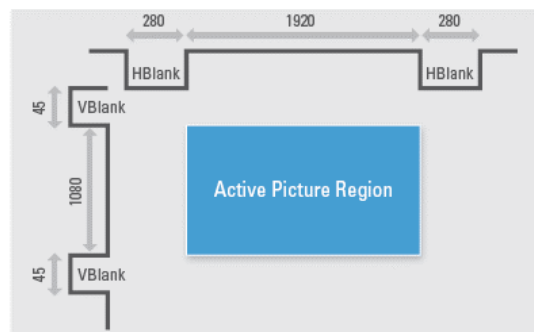


Figure 5: Vertical and Horizontal Blanking



7.8.1 Removing Blanking Lines and Pixels

Blanking lines and pixels should be removed when the video is acquired by the 1500-OEM by manually enter the *Vertical* and *Horizontal Front Porch* settings.

Vertical and Horizontal Front Porch Example (manual blanking entry)

Set the *Vertical Front Porch* (vertical lines of blanking) to 45. Set *Horizontal Front Porch* (horizontal pixels of blanking) to 280.

The screenshot shows the 'Generic Digital Settings' window for a camera. The 'Vertical Front Porch' is set to 45 and the 'Horizontal Front Porch' is set to 280, both indicated by red arrows. Other settings include: AutoFill (dropdown), Height (1080), Width (1920), Resulting Flag Bits (0x1), Bit Depth (8), Input (YUV color selected), Interlaced (unchecked), Byte Swap (unchecked), Invert V-Sync Polarity (unchecked), Invert H-Sync Polarity (unchecked), UBO (unchecked), Sync/Crop (None), Camera Init Code (None), and Options (text field). At the bottom, Big: Height (0), Width (0), Vertical Blanking (0), and Horizontal Blanking (0) are also shown.

Figure 6: Data Valid Not Supported

To determine the blanking of a camera when using a custom camera, or a technical reference manual that shows the vertical and horizontal blanking is not available, use the following procedure:

1. Set *Vertical Front Porch* and *Horizontal Front Porch* to 0.
2. Turn off stabilization (Panel Plus main menu » *Configure* » *Stabilization* » *Disable All Processing*).
3. Disable *AutoChop* for the camera (Panel Plus main menu » *Configure* » *Margin Chopping*).
4. Save the parameters to the board, and then reboot the system. The network video should be viewable in Panel Plus.
5. Point the camera at a bright white scene. Rows at the top or columns at the left that remain gray are blanking areas.
6. Perform an SD card snapshot with Capture as the source. See [EAN-File Recording](#).
7. Download the snapshot and open it in an image viewer application. Zoom in and count the number of blank lines at the top (vertical blanking) and blank columns at the left (horizontal blanking).
8. If an SD Card snapshot cannot be taken, change the horizontal and vertical blanking values. Save the parameters to the board, and then restart the board. View the video in Panel Plus and repeat until all the blanking lines have been removed.

8 Questions and Additional Support

If you are still having issues and require additional support, please contact [Technical Support](#). Additional support, documentation, and Engineering Application Notes (EANs) can be found on the Support pages of the SightLine Applications [website](#).



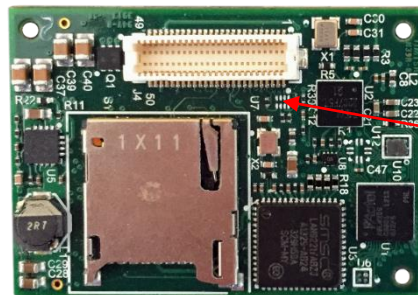
Appendix A - Missing Driver Chip

IMPORTANT: Pre July 2014 builds without U7 chip installed.

Some pre-production REV C (green PCB) boards shipped prior to July 2014 did not have the U7 driver chip installed. These boards will not have I²C capability on J4, which prevents HDMI functionality.



Driver chip installed on board



Driver chip not installed on board (pre-July 2014 builds)

Figure A1: U7 Driver Chip Location

Appendix B - Anti-Alias Filter

The 1500-OEM does not have an anti-aliasing filter, however if aliasing noise is observed, an anti-aliasing filter has been shown to be beneficial in improving video quality. Figure B2 shows the recommended location of anti-aliasing filter input circuit.

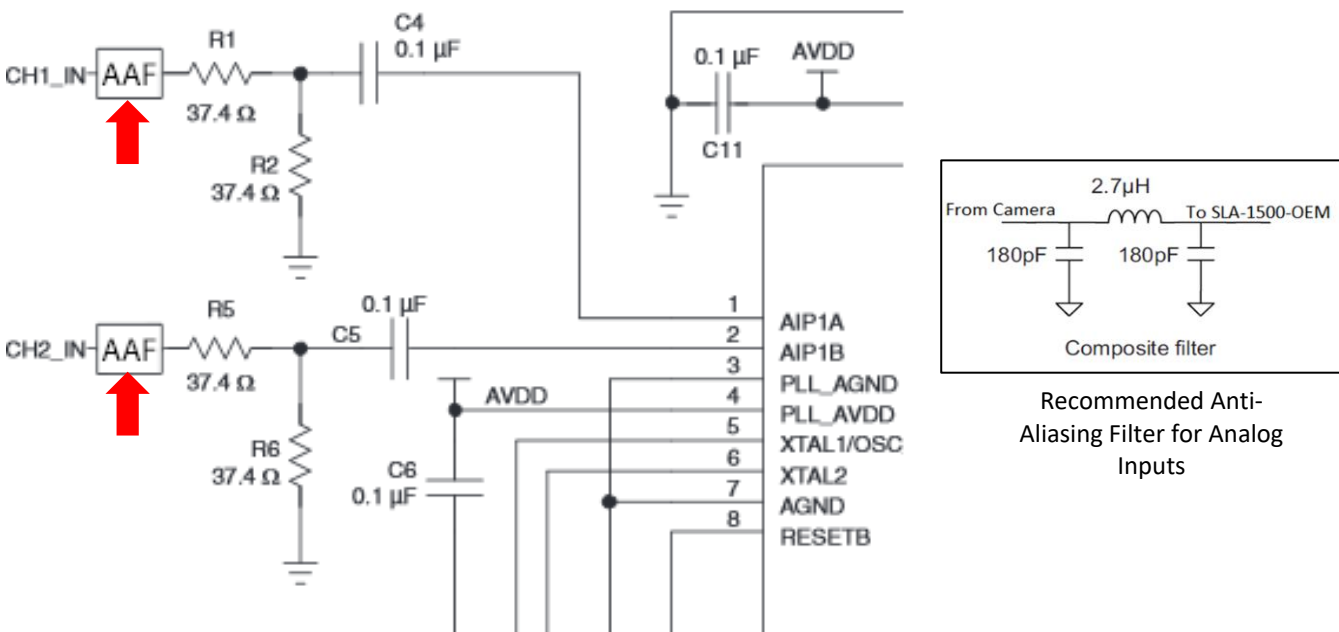



Figure B1: Anti-Aliasing Filter Input Circuit



Appendix C - Analog Input Noise Shielding

 *The analog input connection to the 1500-OEM should use coax or other shielded cable.*

Keeping the analog and AGND wires close together and away from noisy sources (cables carrying digital video) and minimizing cable distance and [ground loops](#) can help.

Twisting the analog and analog ground on the input to the 1500-OEM can be highly effective. In the example setup shown below, shielding was done by twisting the two wires in the center without detaching the pins from the connectors. This keeps the two wires away from noisy sources, i.e., the white flat cable carrying digital video.

Using the analog output of the 1500-OEM connected to an analog monitor will show high frequency noise better than on H.264 compressed network video. This is a more effective setup for testing shielding effects since the change in quality is more apparent.

 *Sending setup pictures to [Support](#) can help identify issues more quickly.*

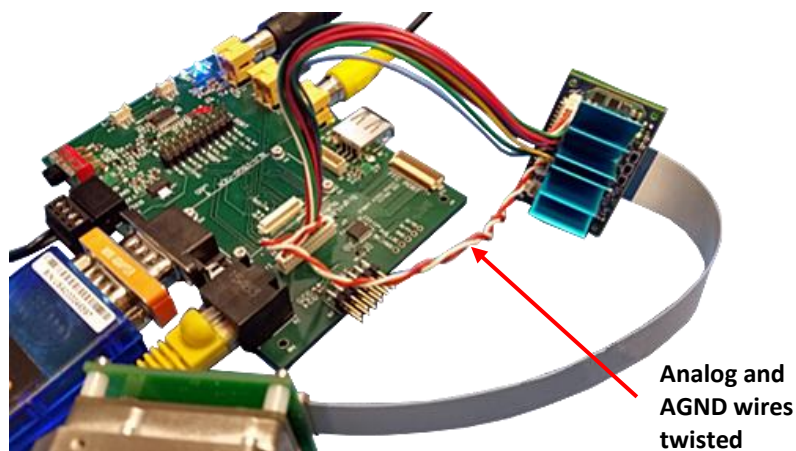


Figure C1: Analog Input Wire Twisting Example



Appendix D - Level Translators

D1 Overview

This section discusses issues that can occur in daisy-chain applications where a bidirectional level translator is on a line that already has a separate bidirectional level translator on the OEM board.

Using back-to-back bidirectional translators can lead to erratic behavior and logic levels within the system causing unintended voltages that exceed design specifications.

The example in this section is using a TXB0104 level translator feeding a SparkFun BOB-12009 level translator. These results can also be typical in other sets of bidirectional level translator applications.

1500-OEM use case scenario:

VIOSEL is tied to a voltage (3.3V) for camera communications, but a different voltage is needed (5V) on lines from J4 (Serial 1) to communicate with a separate piece of equipment such as a lens.

Customers wish to use Serial Port 0 from J3 at a voltage level other than 3.3V.

Recommended associated documents:

[Circuit diagram](#) for the SparkFun logic level bidirectional break out board.

[Texas Instrument TXB0104](#) data sheet.

IMPORTANT: If you are having any issues where a level translator is needed, please contact [Support](#) before performing any modifications to the video processing boards.

D2 Recommended Level Translators

SightLine recommends customers use low-impedance output, unidirectional buffers for their applications. Level translators that use a direction pin to set the direction are also suitable, provided they have a low output impedance and high input impedance.

There are applications where bidirectional level translators can still be used, but it is important to confirm that the signal being translated is not being translated by another bidirectional level translator on the OEM board or an adapter board. To be safe use unidirectional translators wherever possible.

D3 Level Translation Overview

Bidirectional translators are a complicated component. There are many ways that they can be implemented. They rely on one basic principle; they can detect which direction a signal is coming from, and then switch their directions dynamically.

A typical unidirectional translator has a low-impedance output capable of driving LEDs or other significant loads. However, a bidirectional translator with a low-impedance output cannot determine when a load has switched from an input to an output and is trying to drive it, instead of it driving the load.



If a bidirectional translator has a low impedance output, it will result in two outputs connected directly together trying to drive the wire in different directions. This could damage one of the driver stages in the process.

To detect if a signal that was once being driven by the translator has switched directions and intends to drive the translator in the other direction, the bidirectional translator should have a significant output impedance of at least 1k Ω .

In the case of the TXB0108/4 translator example, the output impedance is 4k Ω . In the case of the BOB-12009, in some states it is 10k Ω .

D4 Example: Driving a BOB-12009 with TXB0104

To analyze problems that can arise in this situation, it is important to look at how the BOB-12009 functions. A schematic of the basic level translator block on the BOB-12009 is shown in [Figure D1](#).

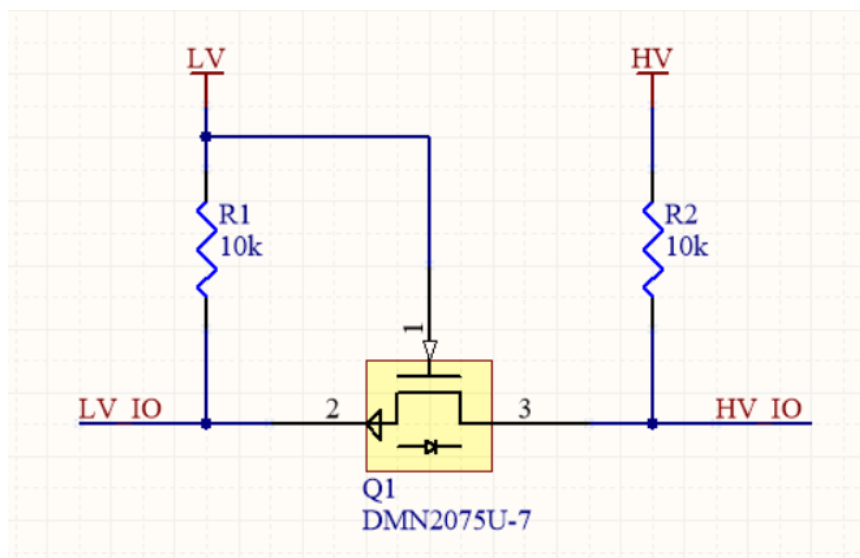


Figure D1: BOB-12009 Basic Level Translator Block

Assume that the LV_IO is driving HV_IO. When LV_IO is high, the mosfet is off, and HV_IO is pulled high by the 10k resistor.

When LV_IO is low, the mosfet is turned on and HV_IO is pulled low through the drain of the mosfet.

In the alternative case, HV_IO is driving LV_IO. When HV_IO is high and LV_IO is low, the mosfet will be turned on. LV_IO will also be pulled high until it turns off. At this point the 10k resistor will pull LV_IO up to where it needs to be.

When HV_IO is low, the body diode of the mosfet will pull LV_IO down until the mosfet starts conducting and then pulls LV_IO further down.

It is important to note that there are some situations where the outputs are being set by a 10k Ω resistor instead of a low-impedance source.



TXB0104 level translator in front of the BOB-12009:

Note what happens when the TXB0104 level translator is placed in front of the BOB-12009. To simplify the circuit, voltage levels can be included for a common scenario - translating the 3.3V up to 5V.

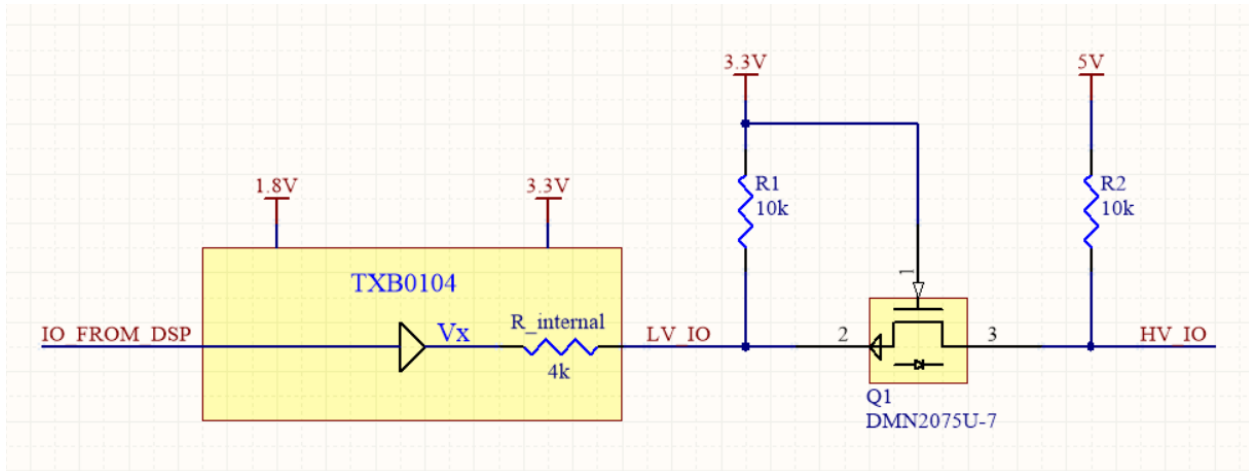


Figure D2: TXB0104 Feeding BOB-12009

In the following example, there is a low-level input (0V) to the TXB0104. 0V is at the internal node V_x on the schematic. A voltage divider has been created by R_1 and R_{internal} . R_2 is passing current from the 5V source.

Ignoring the effects of the mosfet, turned on in this scenario, gives an output voltage of 1.51V for an input voltage of 0V. This is unacceptable as a low-level voltage to a 5V input stage.

It is easy to see how this problem could be resolved by using a low output impedance, unidirectional buffer. This would reduce R_{internal} to $\sim 0\Omega$. It would also be easy to sink the $>1\text{mA}$ current from the two pull-up resistors.

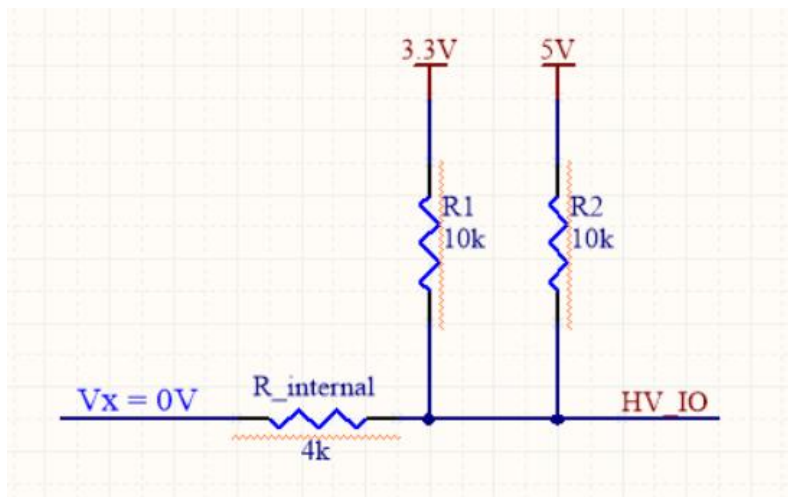


Figure D3: Equivalent Circuit Seen by HV_IO