EAN-LVDS Video Output

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Exports: Export Summary Sheet

EULA: End User License Agreement

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CAUTION: Alerts to a potential hazard that may result in personal injury, or an unsafe practice that causes damage to the equipment if not avoided

IMPORTANT: Identifies crucial information that is important to setup and configuration procedures.

Used to emphasize points or remind the user of something. Supplementary information aids in the use or understanding of the equipment or subject, which is not critical to system use.

1 Overview

This document describes LVDS output on the 1750-OEM. This output is intended to provide raw and NUC corrected 16-bit grayscale data output, as well as corrected 8-bit grayscale output.

ⓘ The settings below are supported in software release 3.6.9 and later.

1.1 Additional Support Documentation

The Panel Plus User Guide provides a complete overview of settings and dialog windows. Accessed from the Help menu of the Panel Plus application.

The Interface Command and Control (IDD) describes the native communications protocol used by the SightLine Applications product line. Also available as a PDF from the Software Downloads page.

Additional Engineering Application Notes (EANs) and ICDs are available on the Documentation page.

1.2 SightLine Software Requirements

See the camera configuration tables for specific OEM Sightline software version requirements for supported cameras.

ⓘ **IMPORTANT:** The LVDS output requires firmware version 3.6.6 or above for the 1750-OEM and Panel Plus.

ⓘ **IMPORTANT:** The Panel Plus software version should match the firmware version running on the board. Firmware and Panel Plus software versions are available on the Software Download page.

2 LVDS Display Supported Output Formats

Currently grayscale output is supported. If the acquisition setting of the camera is not set to one of the following formats, selecting any other format will trigger a user warning when choosing the LVDS display:

- Raw 16-bit grayscale video is supported.
- Raw 16-bit NUC corrected grayscale video is supported when enabling NUC correction through Panel Plus.
- Processed 8-bit grayscale video (NUC and Auto Gain) is supported. This is output in the upper 8-bits of 16-bit LVDS output.
- The 1750-OEM is limited to 16-bits data output to the LVDS display.

3 Supported LVDS Resolutions

The table below shows the supported display resolutions for LVDS display (16/8-bit grayscale, firmware 3.6.9). Enabling other resolutions will trigger a user warning.

Table 1 : Supported LVDS Output Resolutions and Video Timing Parameters

Resolution Name	Width	Height	FPS	Clock MHz	Horizontal Timing (Front porch/sync pulse/back porch/total)	SLA HFP = Back Porch Panel+ Value	Vertical Timing (Front porch/sync pulse/back porch/total)	SLA VFP = Back Porch Panel+ Value
720p30	1280	720	30	74.25	1760/40/**220**/3300	220	5/5/**20**/750	20
720p50	1280	720	50	74.25	440/40/**220**/1980	220	5/5/**20**/750	20
720p60	1280	720	60	74.25	110/40/**220**/1650	220	5/5/**20**/750	20
1080p30	1920	1080	30	74.25	88/44/**148**/2200	148	4/5/**36**/1125	36
640x512p60	640	512	60	25.0	48/32/**64**/784	64	3/7/**5**/527	5
640x512p30	640	512	30	12.500	48/32/**64**/784	64	3/7/**5**/527	5
1280x1024p50	1280	1024	50	75.5	48/32/**80**/1440	80	3/7/**6**/1040	6

4 Video Output Format and Timing Diagram

The LVDS output of the 1750-OEM is designed to operate a monitor using the FPD-Link format for data and timing. FPD-Link is a standard used in automotive applications. FPD-Link systems often convert data from a MIPI camera output, use FPD-Link to transmit it, then convert back into a MIPI signal for display.

FPD-Link shares significant similarities with Camera Link in the following areas:

- Camera link serializes twenty-eight total lines of data, into four lanes. This means the camera link clock is seven times the pixel clock.
- When the camera link signal is decoded, a clock that operates at 1/7 times the frequency of the original clock is also generated. This new clock becomes the pixel clock for the data.
- There are three synchronization lines included in the twenty-eight serialized data lines:
  - FVal – Frame Valid or Vertical Sync
  - LVal – Line Valid or Horizontal Sync
  - DVal - Data Enable (for FPD-Link) or Data Valid (for Camera Link). Data Valid (CL) can indicate that individual pixels are not valid for the video. Data Enable signal (FPD) is high for all valid pixels in a row. The DVal output of the 1750 LVDS output is different from Data Valid as described in the Camera Link specification. See Figure 1

The timing diagram for 720P60 is shown in Figure 1. The timing/blanking values can be correlated with the values shown in Table 1. For other resolutions the format of the data timing is the same and can also be derived from the same table.

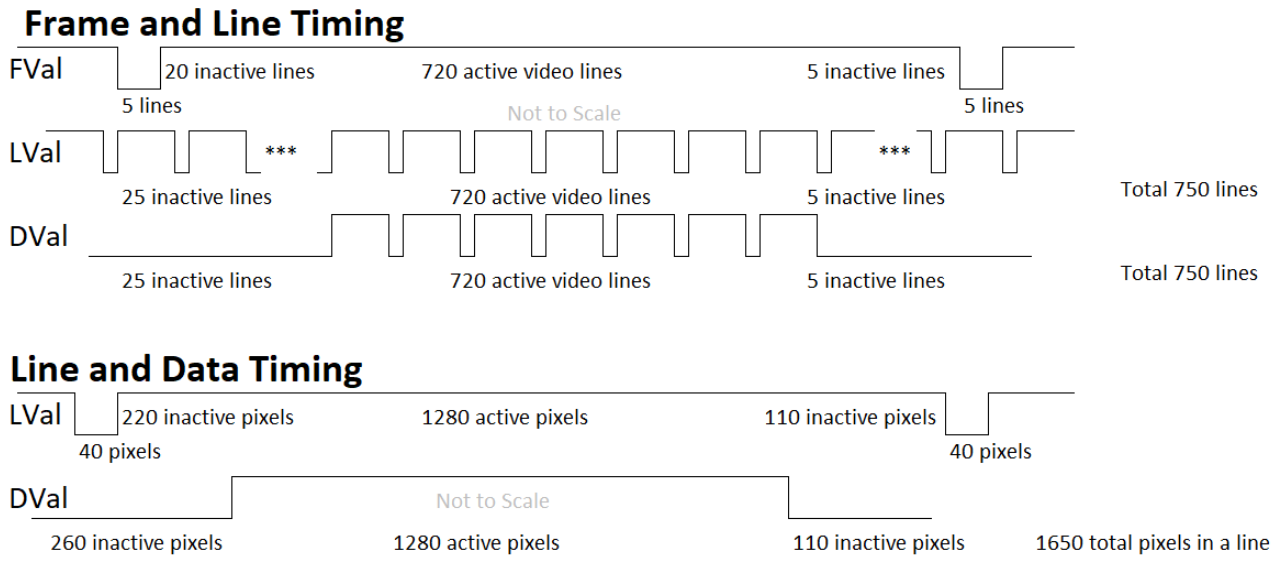

Figure 1: Timing Diagram for 720P60

5 LVDS Capture with Sightline Hardware

The LVDS output can be captured with the 3000-OEM, 4000-OEM and 1750-OEM. This can be done using the 3000-CLK input board.

The capture parameters use 16-bit grayscale input at the same resolution as the LVDS output.

For image alignment either enter the vertical and horizontal porch settings manually or use the *Data_Valid* synch setting to select only active pixels:

- Enter the sightline capture VFP and HFP settings in Table 1.
- Use VFP=HFP=0 and select the *Data_Valid* under the *Synchronization* pull down menu.
- For 640 x 512 and similar resolutions, enter the following options string in the *Acquisition Settings* dialog window in the *Options* field: *fpga=GEN_HD20,mipi_clk=5,mipi_txl=1*

6 LVDS Capture with Customer Designed Hardware

The best approach is to receive and decode SightLine LVDS output with customer designed hardware is to use the same Camera Link DS90CR288A receiver chip that is in SLA-3000-CLK adapter board.

The schematic for the SLA-3000-CLK board is available from SightLine Support. This schematic shows the data ordering and synchronization signal locations.

The output of the 1750 LVDS follows the Camera Link base. Currently this is 16- or 8-bit grayscale.

- 16-bit grayscale is in the low 16 bits D0 to D15
- 14-bit grayscale is in the lower 14 bits D0 to D13
- 8-bit output is in bits D8 to D15
- The FLD signal on the SLA-3000-CLK schematic is Data Valid (or Line Valid)

SightLine LVDS output has been validated with several camera link frame grabbers.

7 Supported Frame Grabbers

The Pleora-CL-U3 Camera Link to USB3 frame grabber has been confirmed to work with the incoming LVDS data. SightLine Support can provide a configuration file for the Pleora eBUS player GUI, which will capture 720P60. This can be modified to work with other supported resolutions by changing the resolutions and X,Y offsets (blanking).

To use the Pleora frame grabber go into settings and make the following changes:

- Disregard DVal. Even if X,Y offsets == 0, enabling Data Valid will result in no video being displayed.
- Use LVal as Level Valid.
  - Enter an X offset of 220 pixels blanking before active video.
- Use FVal as Level Valid:
  - Enter a Y offset with 20 lines of blanking before active video.

The following eBus Player settings have been changed from their default:

<parameter name="Width">1280</parameter>
<parameter name="Height">720</parameter>
*<parameter name="**OffsetX**">220</parameter>*
*<parameter name="**OffsetY**">20</parameter>*
<parameter name="PixelFormat">Mono16</parameter>
*<parameter name="**PixelBusDataValidEnabled**">0</parameter>*
<parameter name="PixelBusDataValidPolarity">High</parameter>
<parameter name="PixelBusLineValidPolarity">High</parameter>
<parameter name="PixelBusFrameValidPolarity">High</parameter>
*<parameter name="PixelBusLineValidEdgeSensitivity">**Level**</parameter>*
*<parameter name="PixelBusFrameValidEdgeSensitivity">**Level**</parameter>*

8 Multiple Display Output Support

Simultaneous LVDS and network display are supported in 3.6.6 software and above. In 3.6.7 software and above simultaneous HDMI, LVDS and network video are supported.

9 Questions and Additional Support

For questions and additional support, please contact SightLine Support. Additional support documentation and Engineering Application Notes (EANs) can be found on the Documentation page of the SightLine Applications website.

Appendix A: Video Timing Scope Snapshots for 720P60

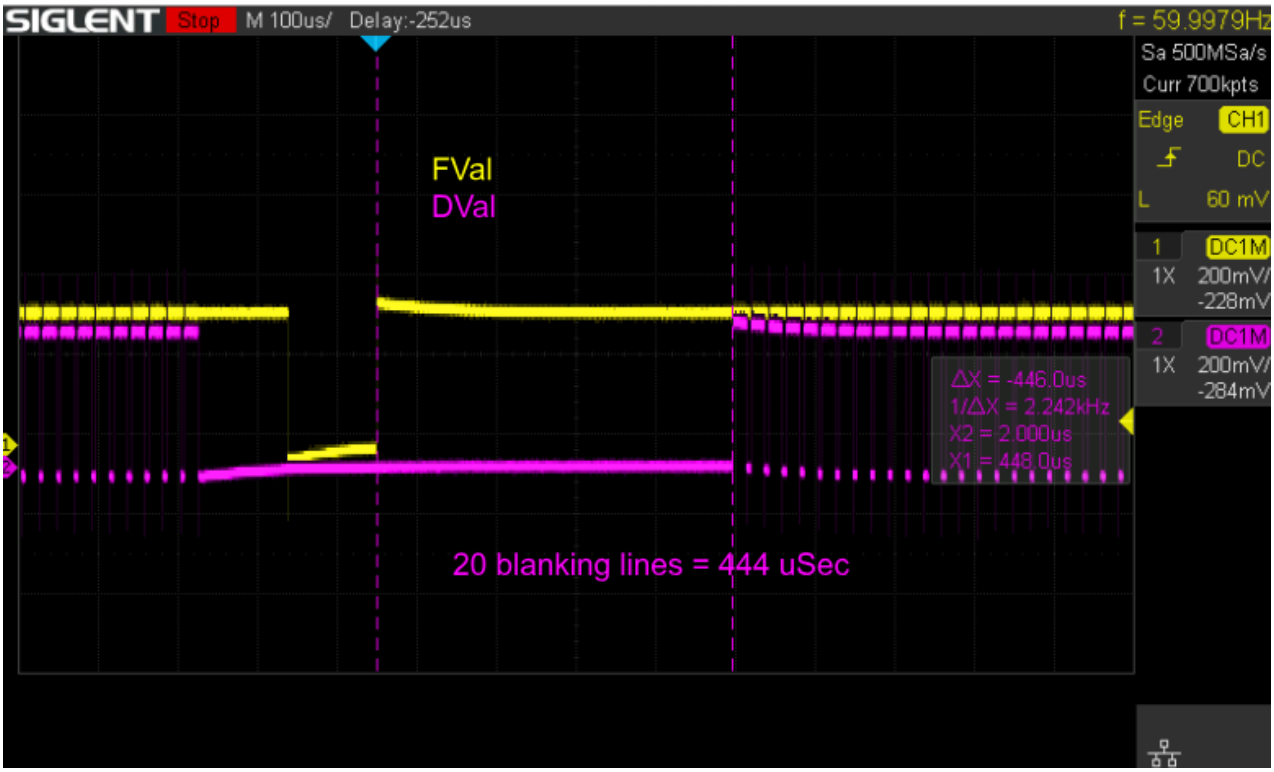

Figure A1: Video Timing Scope - FVal and DVal

Figure A2: Video Timing Scope - FVal and LVal

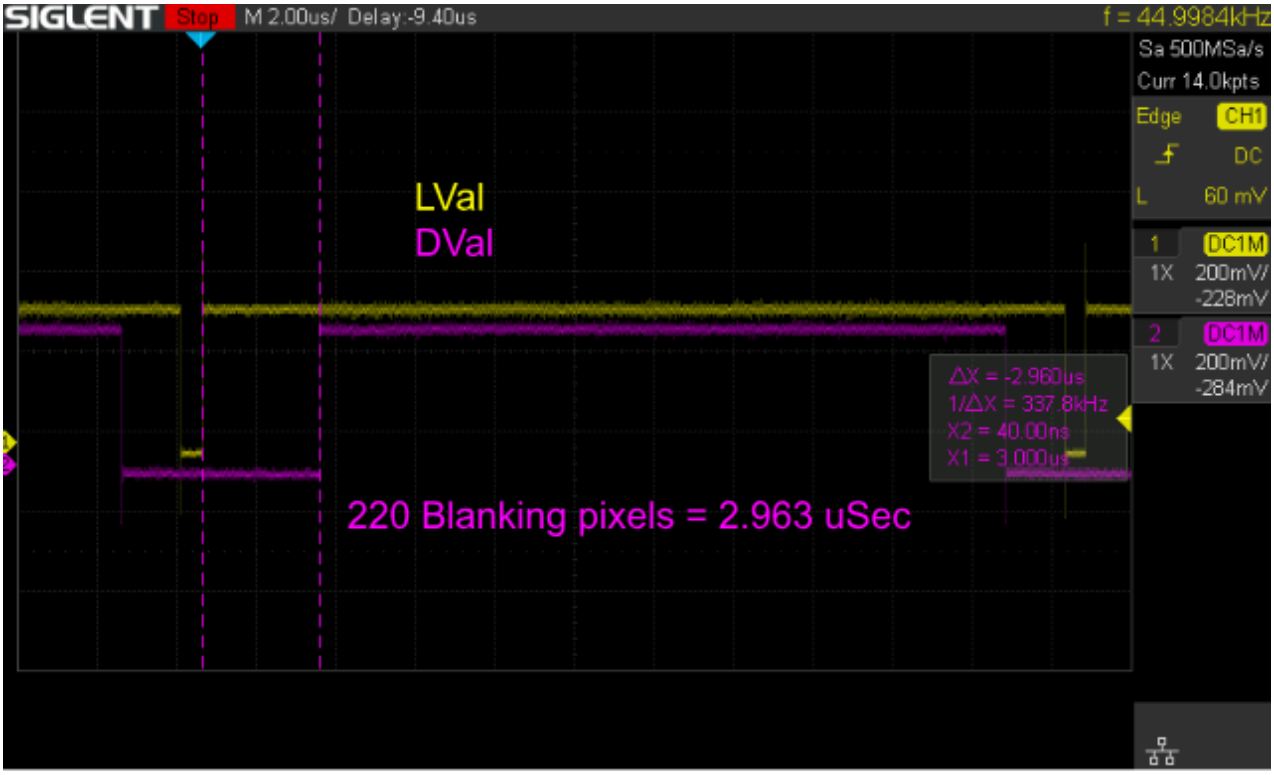

Figure A3: Video Timing Scope - LVal and DVal