SightLine APPLICATIONS

ICD-4000-OEM

PN: ICD-4000-OEM

9/14/2020

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Alerts

The following notifications are used throughout the document to help identify important safety and setup information to the user:

⚠ **CAUTION:** Alerts to a potential hazard that may result in personal injury, or an unsafe practice that causes damage to the equipment if not avoided.

ⓘ **IMPORTANT:** Identifies crucial information that is important to setup and configuration procedures.

Used to emphasize points or reminds the user of something. Supplementary information that aids in the use or understanding of the equipment or subject that is not critical to system use.

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Revision History

Date	Description
9/11/2020	Correct I2C pin designations to match schematic. Add current 400 kHz frequent note to connector J6 pinout table and connector J9 pinout table.
8/24/2020	Corrected Grayscale bit locations in the Connector J6: 3000/4000 Input Board Table.
8/14/2020	Updated J16 HDMI (FFC connector) table - Pin 1 is the same as Pin 2.
7/20/2020	Corrected HDMI Output connecter label in Video Output section.
7/16/2020	Add GPIO numbers to J6 pinout table.
7/8/2020	Added EAN-OEM-Recovery link to 4000-DEBUG section.
6/1/2020	Added maximum width and height of acquired image and ROI.
4/16/2020	Added warning that the 4000 should not be powered through connector J8: USB 3.0 (Type-C).
4/8/2020	Added new section - Customer Designed 4000-OEM Boards and Camera Interface Options.
3/10/2020	FPGA now supports multiple pixel widths in 3.01 software. Added FPGA Video Resolution and Pixel Clock Requirements table for 3.01 software.
1/24/2020	Added max voltage, current and power connector notation to pins 55, 57, 59, 61. Corrected power connector label.
1/17/2020	Added more video format details. Add section on FPGA video resolution requirements.
1/14/2020	Added notes on connector J6 data bit locations.
12/17/2019	Added 4000-OEM STEP file link.
12/14/2019	Correct MIPI board serial ports to 4,6,7. Add link to MIPI board ICD.
11/26/2019	Corrected I2C reference for connector 6 and connector 9 in Connector Descriptions table and Pin 20 and 21 in MIPI Port table.
10/17/2019	Added voltage qualification note to specifications.
9/17/2019	Corrected pins in Serial Port / GPIO table for connector J2.
8/9/2019	Clarification for serial ports. Changed GPIO label to SW labels. Revised heatsink statement.
6/17/2019	Created document.

1 Overview

Describes power requirements, thermal management, interface specifications, and connector pinouts for the 4000-OEM video processing board.

> ⚠ **CAUTION:** Any customer modifications to SightLine OEM and adapter boards will void the warranty and can potentially damage the board. Before attempting any modifications, please contact Support.

1.1 Additional Support Documentation

Additional Engineering Application Notes (EANs) can be found on the Documentation page of the SightLine Applications website.

The Panel Plus User Guide provides a complete overview of settings and dialog windows located in the Help menu of the Panel Plus application.

The Interface Command and Control (IDD) describes the native communications protocol used by the SightLine Applications product line. The IDD is also available as a PDF download on the Documentation page under Software Support Documentation.

1.2 Sightline Software Requirements

Panel Plus software and firmware versions:

4000-OEM requires Panel Plus and Firmware 3.0.0 and higher.

> ⓘ **IMPORTANT:** The Panel Plus software version should match the firmware version running on the board. Firmware and Panel Plus software versions are available on the Software Download page.

2 Safe Device Handling

> ⚠ **CAUTION:** To prevent damage to hardware boards, use a conductive wrist strap attached to a good earth ground. Before picking up an ESD sensitive electronic component, discharge built up static by touching a grounded bare metal surface or approved antistatic mat.

3 4000-OEM Overview

The 4000-OEM has 11 connectors and one micoSD card slot. Connectors are used to connect power, Ethernet, Serial ports, MIPI input, HDMI output, USB3, and digital video in (with the use of a 3000-adapter board).

Figure 1: 4000-OEM Overview

3.1 4000-OEM Specifications

Revision: A3 (Initial Release)

Dimensions: 1.496 in x 1.988 in (38 mm x 50.50 mm)

Weight: Estimate 30 grams

Voltage (VIN): 8 - 16 VDC (12 VDC nom)[1]

Power: 6 W

Drawing: 4000-OEM

STEP File: 4000-OEM Rev A STEP

All 4000-OEM board mounting holes support M2 screws.

Table 1: Hardware Revisions

Board Revision	Changes
Rev A	Initial Release

3.2 Interface Protocol

The 4000-OEM shares the same interface protocol as other SightLine video processing boards. The protocol is a packet-based command and control interface.

[1] A slightly extended input voltage range is possible with some tradeoffs. Contact Support for more information if this is relevant to your application

3.3 Functional Block Diagram

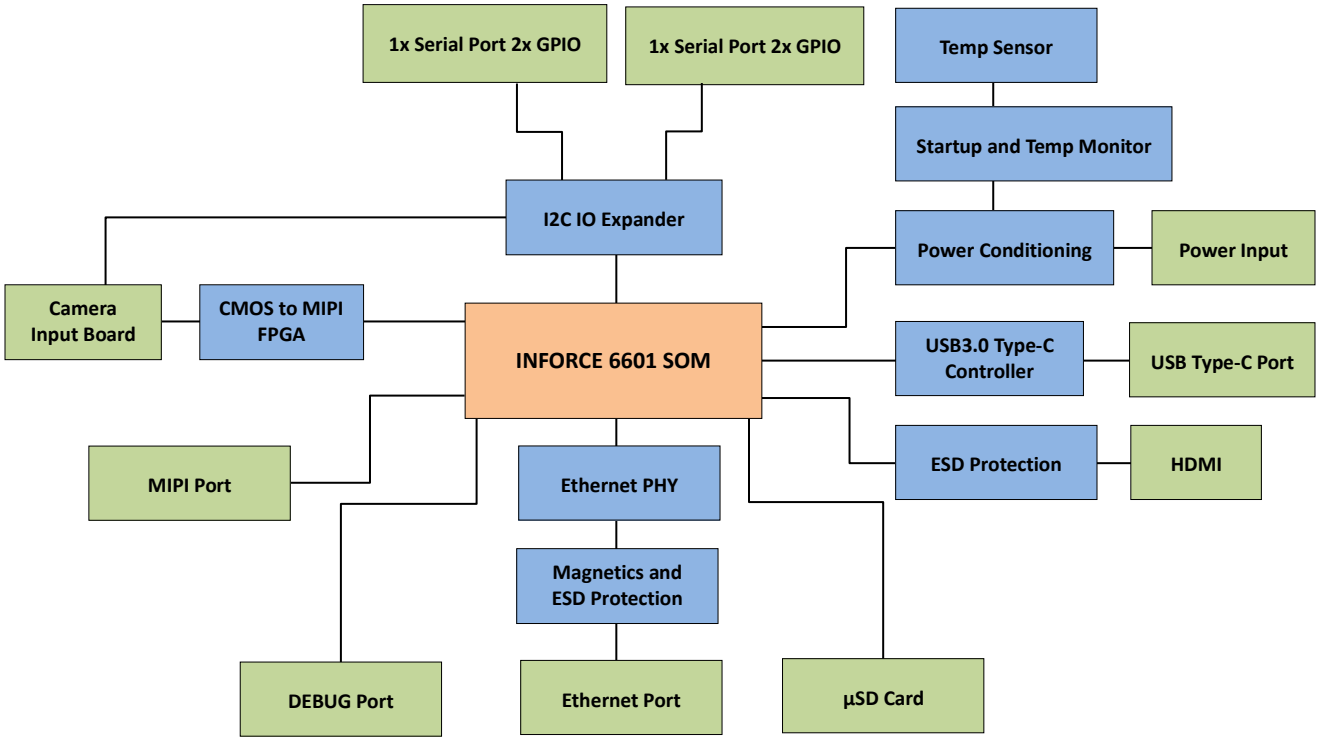

Figure 2: 4000-OEM Hardware Block Diagram

3.4 Design Checklist

- ✓ Provide a sufficient heat sink for the Snapdragon 820 processor and other major components
- ✓ Expose serial port 0 (on J25) to an accessible connector for debugging
- ✓ Expose Ethernet port (on J4) to an accessible connector for debug, command and control, and firmware update capability
- ✓ Serial ports 0 through 3 can be configured for command and control, otherwise use Ethernet port.
- ✓ All serial ports are 3.3V TTL levels (unless otherwise noted)

4 Thermal Management

4.1 Heatsink Guidelines

The component temp range for the InForce 6601 SOM and the Ethernet PHY are 0°C to 70°C, all other components temp range is -40°C to 85°C. All hardware requires some form of mechanical heatsink.

The 4000-OEM typical power consumption is less than 6W @ 12V.

Most customers design a heatsink in conjunction with their system integration effort that provides a direct conducted path to a significant thermal mass (typically the wall of a gimbal or housing). Others use active cooling (for example fans) as part of the design.

The internal temperature as reported in Sightline Application Panel Plus not to exceed +85°C (185°F) or the system will start to reduce clock speed, and eventually shut down.

STEP files for the heatsink interface are available from SightLine that can help with heatsink design and integration.

4.2 Gap Pads

Use some form of thermally conductive material for filling gaps between the hot components and the heat sink. Examples such as the TGlobal TG6050 Ultra Soft Thermal Conductive Pad (6W/mK or higher) are recommended. Do not use gap pads in conjunction with thermal grease.

5 Ports, LED, GPIO and Sensors

5.1 LED Summary

Label	Color	Function
D1	Green	Board Power
D3	Green	IO Expander User LED, GPIO15
D5	Amber	Ethernet PHY Link Indicator

5.2 Serial Port Summary

All serial ports are 3.3V TTL. When using a SightLine mezzanine board with a 3-pin connector, use the CAB-03xx for easy break out to either a pig tail, Molex-to-Molex, or DB-9 connector.

Table 2: 4000-OEM Serial Port Summary

Name	Connector	Notes
Serial Port 0	J25 P1-3	General Purpose (SLA Command)
Serial Port 1	J2 P1-3	General Purpose
Serial Port 2	J6	Camera interface use only
Serial Port 3	J25 P4-7	General Purpose

Additional Serial ports are available when attaching an SLA-4000-MIPI board to the MIPI port on J9 (serial ports 4, 6, and 7). See the SLA-4000-MIPI section in the ICD-3000-4000 Adapter Boards.

A debug serial port is exposed on J7 P7-8 and should be used for debugging only. Debug serial port is 1.8V TTL.

5.3 GPIO Summary

GPIOs are used to identify the Input Mezzanine Board Address attached to connectors J6 (4000-OEM) or J9 (J10 on SLA-4000-MIPI board). See the current list of IDs and more general-purpose IO details in Connector Descriptions.

6 Connector Descriptions

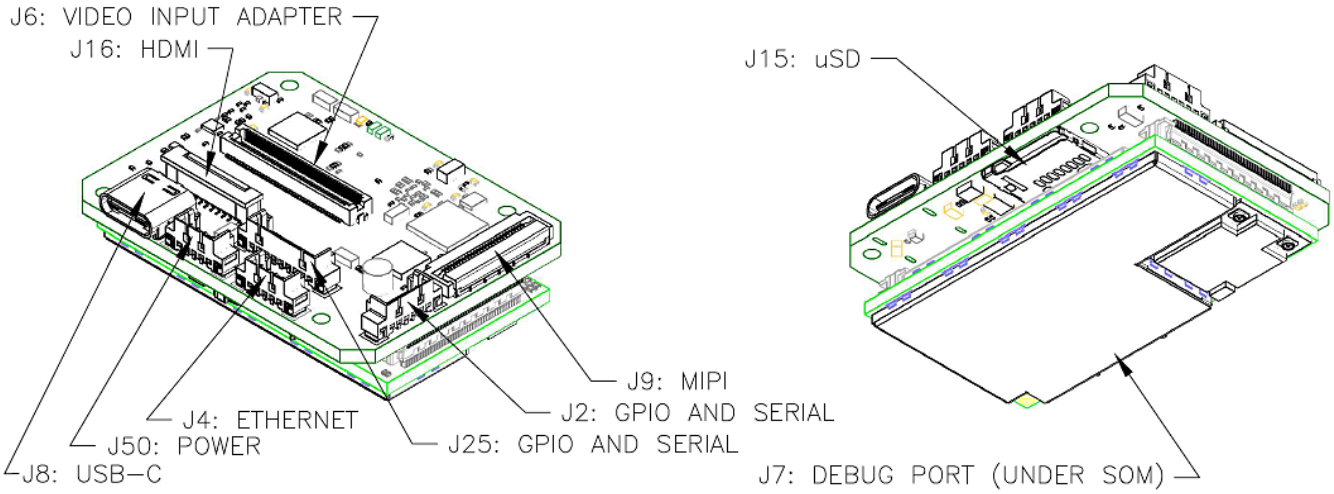

Figure 3: 4000-OEM Connector Descriptions

Table 3: Connector Descriptions

Connector	Description
J2: Serial Port / GPIO	Serial port 1, GPIO_459, GPIO_460
J4: Ethernet	Ethernet 10/100Mbps
J6: 3000/4000 Video Adapter Input	Digital video in 0, serial port 2, I2C-1, GPIO
J7: Recovery / Debug*	System recovery and debug serial port
J8: USB 3.0	USB 3.0 (type C)
J9: MIPI Port	MIPI Port, I2C-3 (Digital Video in 1, serial ports, w/adapter board)
J15: MicroSD slot	MicroSD card slot
J16: HDMI Output	HDMI Output (FFC)
J25: Serial Port / GPIO	Serial port 0 and 3, GPIO_458, GPIO_125
J50: Power Connector	Typical 12VDC (see 4000-OEM Specifications for min/max)
S2: IO2 SOM	INFORCE SOM
S3: IO1 SOM	INFORCE SOM

**The debug serial port is exposed on J7 P7-8 and should be reserved for debugging only. Debug serial port is 1.8V TTL.*

⚠ **CAUTION:** J4 (Ethernet) and J50 (power) are adjacent 4-pin connectors. **DO NOT** connect power to the Ethernet port. Connecting power to the Ethernet port **will** damage the board.

6.1 Ethernet

On connector J4, pin 1 through pin 4 represent the Ethernet connection. It supports 10/100BASE-T only.

TXA_P/TXA_N is sending information from Sightline the sightline board, TXB_P/TXB_N is receiving.

Ethernet magnetics and Ethernet protection: The 4000-OEM is configured with onboard Ethernet magnetics and ESD protection. It meets the following IEC standards, IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact) IEC 61000-4-4 (EFT) 40A (5/50ns) IEC 61000-4-5 (Lightning) 40A (8/20µs).

6.2 Connector J6: 3000/4000 Input Board

Connector: DF12(3.0)-80DP-0.5V(86) Mates with: DF12(3.0)-80DS-0.5V(86)

Column key for notes column below (data bit locations):

Y = luminance **CbCr** = Chrominance **G** = Grayscale bits

Table 4: 4000-OEM (J6) Pinout

Pin	Description	Notes	Pin	Description	Notes
2	NC		1	VIN_**A**CLK	Pixel Clock
4	Ground		3	Ground	
6	VIN_D22		5	VIN_D23	
8	VIN_D20		7	VIN_D21	
10	VIN_D18		9	VIN_D19	
12	VIN_D16		11	VIN_D17	
14	Ground		13	Ground	
16	VIN_D14	**Y**6, **G**14	15	VIN_D15	**Y**7, **G**15
18	VIN_D12	**Y**4, **G**12	17	VIN_D13	**Y**5, **G**13
20	VIN_D10	**Y**2, **G**10	19	VIN_D11	**Y**3, **G**11
22	VIN_D8	**Y**0, **G**8	21	VIN_D9	**Y**1, **G**9
24	Ground		23	Ground	
26	VIN_D6	**CbCr**6, **G**6	25	VIN_D7	**CbCr**7, **G**7
28	VIN_D4	**CbCr**4, **G**4	27	VIN_D5	**CbCr**5, **G**5
30	VIN_D2	**CbCr**2, **G**2	29	VIN_D3	**CbCr**3, **G**3
32	VIN_D0	**CbCr**0, **G**0	31	VIN_D1	**CbCr**1, **G**1
34	Ground		33	Ground	
36	NC		35	NC	
38	NC		37	NC	
40	NC		39	NC	
42	Port ID (out)	See pin notes	41	NC	
44	Ground		43	Ground	
46	NC		45	VIN_HSYNC	Horizontal Sync
48	NC		47	VIN_VSYNC	Vertical Sync
50	NC		49	VIN_FLD	Field
52	NC		51	VIN_DE	Optional
54	Ground		53	Ground	
56	Passthrough ground		55	Passthrough VIN	See J50*
58	Passthrough ground		57	Passthrough VIN	See J50*
60	Passthrough ground		59	Passthrough VIN	See J50*
62	Passthrough ground		61	Passthrough VIN	See J50*
64	Ground		63	Ground	
66	TX2	3.3V TTL	65	RX2	3.3V TTL
68	BLSP8_I2C _SDA	I2C-1	67	BLSP8_I2C _SCL	I2C-1 (400 kHz)
70	GPIO1_3000_BRD	GPIO_453	69	GPIO0_3000_BRD	GPIO_452
72	GPIO3_3000_BRD	GPIO_455	71	GPIO2_3000_BRD	GPIO_454
74	GPIO5_3000_BRD	GPIO_457	73	GPIO4_3000_BRD	GPIO_456
76	+3.3V (out)		75	+3.3V (out)	
78	Ground		77	Ground	
80	+1.8V (out)		79	+1.8V (out)	

**Max voltage = VIN (See Specifications and connector J50) Max current = 1.2A*

6.3 Connector J2: Serial Port / GPIO

Connector: Molex 5POS, 53398-0571 Mates with: Molex 5POS Housing, 51021-0500

Table 5: Serial Port / GPIO

Pin	Signal	Description
1	GND	
2	TX1	3.3V TTL
3	RX1	3.3V TTL
4	GPIO_459	GPIO (4000-OEM schematic net name GPIO7_USER)
5	GPIO_460	GPIO (4000-OEM schematic net name GPIO8_USER)

6.3.1 Serial Ports

On connector J2, serial port 1 (TX1, RX1) are 3.3V TTL Voltage levels

6.4 Connector J25: Extra Serial / GPIO

Connector: Molex 8POS, 53398-0871 Mates with: Molex 8POS Housing, 51021-0800

Table 6: Extra Serial/GPIO

Pin	Signal	Description
1	GND	
2	TX0	3.3V TTL
3	RX0	3.3V TTL
4	GND	
5	TX3	3.3V TTL
6	RX3	3.3V TTL
7	GPIO_458	GPIO (4000-OEM schematic net name GPIO6_USER)
8	GPIO_125	Default MCU_PB3 Open Drain (Heater control). APQ_GPIO_125 optional w/ resistor load for fan, etc.

6.4.1 Serial Ports

On connector J25, serial port 0 and 3 (TX0/RX0, TX3/RXC3) are 3.3V TTL Voltage levels.

6.5 Connector J4: Ethernet 10/100

Connector: Molex 4POS, 53398-0471 Mates with: Molex 4POS Housing, 51021-0400

Table 7: Ethernet

Pin	Signal	Description
1	TXA_P	TX+
2	TXA_N	TX-
3	TXB_P	RX+
4	TXB_N	RX-

6.6 Connector J16: HDMI (FFC connector)

Connector: Amphenol 20POS, 62674-201121ALF Mates with: Sightline Cable SLA-CAB-HD10

Table 8: HDMI

Pin	Description	Pin	Description
2	HDMI_C_5VOUT	1	HDMI_C_5VOUT
4	HDMI_C_DATA	3	HDMI_C_HPD
6	HDMI_C_CEC	5	HDMI_C_CLK
8	GND	7	GND
10	HDMI_TMDS_CLK_C_P	9	HDMI_TMDS_CLK_C_N
12	HDMI_TMDS_TX0_C_N	11	GND
14	GND	13	HDMI_TMDS_TX0_C_P
16	HDMI_TMDS_TX1_C_P	15	HDMI_TMDS_TX1_C_N
18	HDMI_TMDS_TX2_C_N	17	GND
20	GND	19	HDMI_TMDS_TX2_C_P

6.7 Connector J9: MIPI Port (FFC connector)

Connector: Hirose 28POS, FH41-28S-0.5SH(050) Mates with Sightline Cable SLA-CAB-MIPI-02

Table 9: MIPI Port

Pin	Description	Pin	Description
2	D4+	1	GND
4	GND	3	D4-
6	D3-	5	D3+
8	CLK+	7	GND
10	GND	9	CLK-
12	D2-	11	D2+
14	D1+	13	GND
16	GND	15	D1-
18	IO_HOST_OUT0	17	IO_HOST_OUT1
20	CCIO_I2C_SCL (I2C-3, 400 kHz)	19	GND
22	GND	21	CCIO_I2C _SDA (I2C-3)
24	IO_HOST_IN0	23	IO_HOST_IN1
26	VCC_5V	25	VCC_5V
28	GND	27	VCC_5V

Max power *output over FFC Cable = 6.75W (uses 90% of rated value) at 5V*.

6.8 Connector J7: 4000-DEBUG

Connector: Molex 8 POS, 53398-0871 Mates with: Molex 8 POS Housing, 51021-0800

Table 10: 4000-DEBUG

Pin	Description	Pin	Description
2	USB3_P0_HS_D_P	1	USB3_P0_HS_D_N
4	uUSB_VBUS	3	GND
6	VOL_N	5	QFIL_USB_SELECT
9	BLSP8_UART_RX (1.8V)	7	BLSP8_UART_TX (1.8)

See the 4000-DEBUG section for more information.

6.9 Connector J8: USB 3.0 (Type-C)

Connector: Molex, 1054500101 Mates with: USB Type-C Cable

Table 11: USB 3.0

Pin	Description	Pin	Description
A1	GND	B1	GND
A2	USB3_TX1_N	B2	USB3_TX2_P
A3	USB3_TX1_N	B3	USB3_TX2_N
A4	P5V	B4	P5V
A5	CC1	B5	CC2
A6	USB3_P1_HS1_D_P	B6	NA
A7	USB3_P1_HS1_D_N	B7	NA
A8	NA	B8	NA
A9	P5V	B9	P5V
A10	USB3_RX2_N	B10	USB3_RX1_N
A11	USB3_RX2_P	A11	USB3_RX1_P
A12	GND	A12	GND

CAUTION: Do not power the 4000-OEM board through the USB connector. Damage to the board may occur.

6.10 Connector J50: Power Connector

Connector: Molex 4POS, 53398-0471 Mates with: Molex 4POS Housing, 51021-0400

Table 12: J50 - Power Connector

Pin	Description	Description
1	VIN	Typical 12VDC (see Specifications for min/max)
2	VIN	
3	GND	
4	GND	

7 Video Output Port Description

7.1.1 Signal Levels

Unless otherwise specified, all video signal levels are 3.3 Volts. See the table in the Input Mezzanine Board Address section for example video card accessories.

7.1.2 Power

There are multiple rails available on the connectors to power a mezzanine board or accessories. On the 3.3V rail, do not exceed 0.8A. On the 1.8V rail, do not exceed 0.7A.

7.2 Video Output

HDMI Output (J16):

HDMI 1.3a (TBD 1.4a) compliant interface.

The HDMI output format is specified by the resolution and format specified through Panel Plus. The HDMI output ignores any EDID HDMI format information in the external HDMI sink device.

8 Video Input Port J6 Description (Cam 0)

8.1 Adapter boards

When acquiring video, a set of adapter boards are available to convert popular video signals to parallel digital video for input to the J6 video input port. For specific details see ICD-3000-4000 Adapter Boards.

Input boards examples:

- Sony serial digital interface (Sony FCB cameras and compatible Tamron cameras)
- HD-SDI camera interface
- HDMI camera interface
- Camera Link camera interface
- Hitachi camera interface
- Analog video (NTSC and PAL)

Additionally, parallel video can be acquired using an adapter board that accepts an FFC and FPC cable types. Mating adapter boards are available that attach to specific camera types (Boson, Airborne, etc.)

For custom 4000-OEM board configurations, the information in this section can be used to specify the timing and signals required from the camera interface to the corresponding J6 pin connections. See Customer Designed 4000-OEM Boards.

8.2 Signal Levels and Lattice Crosslink FPGA

Unless otherwise specified, all video signal levels are 3.3 Volts. See the table in the Input Mezzanine Board Address section for example video card accessories.

The maximum input frequency of the pixel clock is 150MHz.

Pixel data should be valid on the rising edge of the pixel clock.

8.3 Supported Standards

Signal locations are outlined in the notes column of the table in 4000-OEM (J6) Pinout.

Unlike the 1500-OEM and 3000-OEM, the 4000-OEM has limitations on the supported resolutions, see section Resolution and Pixel Clock Requirements.

16-bit YCbCr 4:2:2

- 8-bit luminance acquired in signal locations Y0->Y7
- 8-bit chrominance in signal locations CbCr0->CbCr7
- Progressive video only

20-bit YCbCr 4:2:2

Use upper 8-bits of 10-bit data for both Y and CbCr

8-bit BT.656

- Single BT.656: Camera input is supported on each Cam 0 Vin1 Cam 1.
- 8-bits BT.656: Data on signal pins 15->22 (15 = most significant bit) with pixel clock on VIN_ACLK
- 10-bit BT.656: Wire the upper 8-bits of 10 into the above locations. This will contain the most significant video data, as well as the SAV and EAV codes.
- Currently only interlaced BT.656 video is supported (PAL or NTSC)

8.4 Grayscale Camera Data

Up to 16-bit (see 4000-OEM (J6) Pinout)

8-bit data in signal locations G0 → G7 (G8 → G15 should be tied low)

14-bit data in signal locations G0 → G13 (G14 → G15 should be tied low)

16-bit data in signal locations G0 → G15

Discrete sync signals in signal locations VIN_HSYNC, VIN_VSYNC, VIN_ACLK, VIN_FLD, VIN_DE (where x is 0,1)

8.5 Synchronization Signals

The following synchronization signals are used. VIN refers to VIN or VIN1 depending on video input 0 or 1.

- VIN_VSYNC vertical sync: A rising edge (default) indicates the start of a new frame. This can be configured through acquisition parameters to falling edge.
- VIN_HSYNC horizontal sync: A rising edge (default) indicates the start of a new line. This can be configured through acquisition parameters to falling edge.
- VIN_ACLK pixel clock: Pixel data is sampled on the rising edge. Maximum input rate is 74.25 MHz. Clock edge is not currently configurable through acquisition parameters.
- VIN_FLD: The 4000 does not support Field information. MIPI image type does not provide for an *Interlaced* flag in the MIPI packet header. For BT.656 (analog video) inputs the SLA-4000 FPGA takes the interlaced data in BT.656 and generates a progressive frame with 2 fields per frame, then *de-fields* these frames in our processing step. This is not currently supported for other formats (e.g.1080i is not supported)
- VIN_DE: This is line enable or line valid. This is not currently supported by the SLA-4000.

8.6 Resolution and Pixel Clock Requirements

8.6.1 Width Requirements

There are multiple FPGA versions. Each one is specific to a linewidth in pixels, and to a number of bytes in data stream. This is because a packet header is needed for each line in the MIPI packet data. This header width is not dynamically changeable in the current programming interface (Lattice DPhy interface). It must be compiled in. The FPGA version is selected based on width and bytes in the acquisition settings. See the FPGA Video Resolution and Pixel Clock Requirements table.

With the release of 3.01 software the specific FPGA version requirement for different widths of video is no longer needed for Color HD cameras. There are still different versions based on pixel clock rate. This allows customers to use a variety of camera resolutions without the need for SightLine to generate FPGA versions with custom resolutions.

8.6.2 Pixel Clock Requirements

Since the Lattice DPhy interface PLL has a limited lock range, see the frequency in table FPGA Video Resolution and Pixel Clock Requirements for each version. Due to the limitations of the PLL the minimum input pixel clock is 24 MHz. This limitation is currently being addressed by modifying the FPGA code to duplicate pixel values to support lower pixel clock rates. Contact sightline support for details.

The pixel clock rate is used to setup a parameter in the MIPI receiver on the 4000-SOM to allow it to acquire MIPI video. This does not need to be the exact clock rate, but it should be approximate.

8.6.3 Width and Height Requirements

Both the width and height must be multiples of 8.

Table 13: FPGA Video Resolution and Pixel Clock Requirements (Release 3.0)

Video format (FPGA Version)	Width in Pixels	Number Bytes	Pixel Clock MHz
1080P30	1920	2	74.25
720P60/30	1280	2	74.25
BT.656 (Analog)	720	1	27
640 (Boson 16 bit)	640	2	27
640 (Boson 8 bit)	640	1	27

Table 14: FPGA Video Resolution and Pixel Clock Requirements (Release 3.01)

Video format (FPGA Version)	Width in Pixels	Number Bytes	Pixel Clock MHz
1080P60/30	1920	2	148.25
720P60/30	1280	2	74.25
BT.656 (Analog)	720	1	27
640 (Boson 16 bit)	640	2	27
640 (Boson 8 bit)	640	1	27

In 3.01.xx software, 1080P and 720P use the same version of FPGA code. HD color and HD IR cameras will use this same version as well.

8.7 Maximum Width and Height

The capture width and capture height are limited to 4112 x 3040. The processed ROI is limited to 4K 3840 x 2160. The ROI can be moved around in the full image by changing the col and row.

8.8 External Camera Power From OEM

There are multiple rails available on the connectors to power a mezzanine board or accessories. Do not exceed 0.8A on the 3.3V rail. Do not exceed 0.7A on the 1.8V rail.

9 MIPI Port J9 (Cam 1)

The MIPI port provides an interface for directly connecting MIPI cameras to the 4000-OEM. This port provides camera power and camera configuration through I2C. The MIPI port can also be used to connect SightLine HDMI, Sony, and HD-SDI adapter boards through the 4000-MIPI adapter board. The 4000-MIPI board provides a connection to the adapter board and a MIPI FFC cable connection to the J9 MIPI port. For details on supported MIPI cameras and formats see EAN-4000-OEM-MIPI-Cameras.

10 Camera Naming Convention

Connector	Appears in software as:
J6 (3000-Adapter board required)	Camera 0 (Cam 0)
J9 (MIPI)	Camera 1 (Cam 1)
J8 USB3 (USB camera)	Camera 2 (Cam 2)
J8 USB3 (USB camera)	Camera 3 (Cam 3)

11 Power Supplies

ⓘ **IMPORTANT:** The supply voltage level must be compatible with camera adapter board and connected cameras. For example, the 3000-Sony camera adapter board passes supply voltage directly to the attached camera. A Sony EH series camera can only support 6V - 12V. This would limit the supply voltage to the 4000-OEM to this range.

12 Input Mezzanine Board Address

Each of SightLine's camera adapter boards is assigned a unique adapter ID to simplify setup and configuration. This applies to any board connected to J6 (4000-OEM) or via J9 (J10 on the SLA-4000-MIPI adapter board). Use 10k Ohm resistors to pull up (bit value 1) or pull down (bit value 0) to set the address.

In the future, camera configuration will be overwritten in software using SightLine's Command and Control Protocol. If designing a custom camera board to connect to the 4000-OEM, contact SightLine Applications to discuss the correct board address to use.

Table 15: 3000-OEM Mezzanine Board ID Table

Board ID	72	71	70	69	Board Description	Part Number
0x0	0	0	0	0	No board	(Default) No board connected. No video acquired.
0x1	0	0	0	1	Sony block adapter	SLA-3000-Sony
0x2	0	0	1	0	Camera Link® adapter	SLA-3000-CL
0x3	0	0	1	1	Analog video adapter	SLA-3000-AB (Dual analog)
0x4	0	1	0	0	HDSDI adapter	SLA-3000-HDSDI Input
0x5	0	1	0	1	Hitachi adapter	SLA-3000-HITACHI
0x6	0	1	1	0	FFC/FPC adapter	SLA-3000-FFC, SLA-3000-FPC
0x7	0	1	1	1	HDMI camera	SLA-3000-HDMI
0x8 – 0xC	-	-	-	-	Reserved	
0xD	1	1	0	1	Generic adapter	Generic adapter board *
0xE	1	1	1	0	Special custom board	Do not use
0xF	1	1	1	1	*Reserved for future use*	

* *For Generic Adapter ID (0xD) the GPIO pins must be pulled to 0xD by the adapter board. For customer designed adapter boards that copy the SLA adapter board schematics, make sure any decoder or other adapter hardware is enabled with the GPIO pins at 0xD. It is common for SLA designed adapter boards to repurpose these GPIO pins once the board ID is read. The same cannot be assumed for generic adapter boards.*

13 4000-DEBUG

The 4000-DEBUG board provides additional interfacing and software debugging capabilities for the 4000-OEM. It gives the developer access to a debug serial port at RS-232 level, a USB programming/debugging port, and a switch/button combination for board recovery.

13.1 Specifications

Revision: A

Dimensions: 1.71 in x 0.96 in (43.4 mm x 24.4 mm)

Weight: 4.5 grams

Voltage: 5V DC, via USB or external power supply

Power < 5 mW

EANs: EAN-OEM-Recovery

Drawing: TBD

Rev History: A: Initial production release

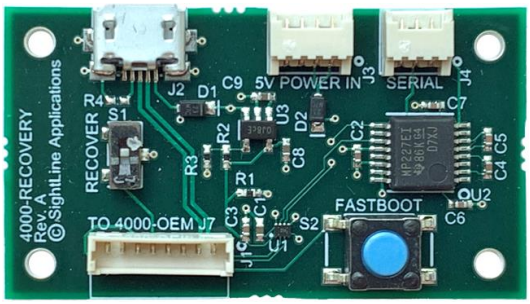

Figure 4: 4000-DEBUG

13.2 Hardware Overview

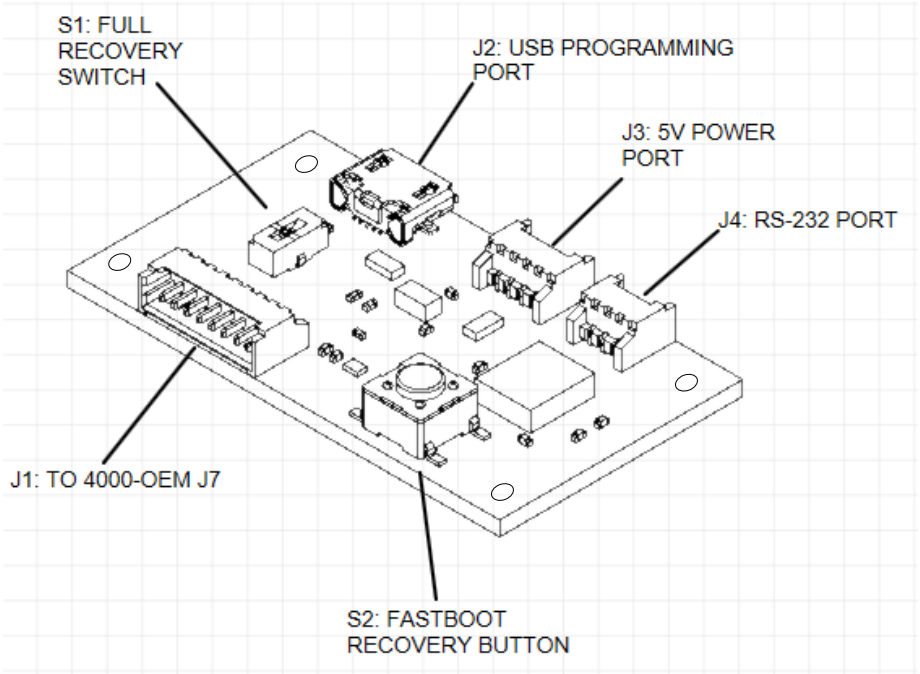

Figure 5: 4000-DEBUG Connector Callouts

Table 16: SLA-4000-DEBUG Board Connector Summary

Label	MFG / MFG Part Number	Function	Mates with:
J1	Molex 53048-0810	To 4000-OEM J7 programming and recovery port	SLA-CAB-XXXX Molex 51021-0800 (housing) and 0500588000 (terminals)
J2	Amphenol 10118192-0001LF	USB programming port	USB Micro-B to USB-A (PC)
J3	Molex 53048-0410	Power (5 V nominal)	SLA-CAB-1505 Molex 51021-0400 (housing) and 0500588000 (terminals)
J4	Molex 53048-0310	Serial debug - RS232 level	SLA-CAB-0303 Molex 51021-0300 (housing) and 0500588000 (terminals)

Table 17: 4000-DEBUG Board Connector Descriptions

Connector	Pin Descriptions	
Connector J1: To 4000-OEM J7 Programming and Recovery port	**Pin**	**Pin Description**
	1	USB3_P0_HS_D_N
	2	USB3_P0_HS_D_P
	3	GND
	4	USB_VBUS (+5V)
	5	FULL_RECOVERY (Switch S1)
	6	FASTBOOT_RECOVERY (Button S2)
	7	BLSP8_UART_TX
	8	BLSP8_UART_RX
Connector J2: USB Programming port	**Pin**	**Pin Description**
	1	USB_VBUS (+5V)
	2	USB3_P0_HS_D_N
	3	USB3_P0_HS_D_P
	4	ID
	5	GND
	6	M1
	7	M2
Connector J3: Power	**Pin**	**Pin Description**
	1	+5V Supply
	2	+5V Supply
	3	GND
	4	GND
Connector J4: Serial Debug Port	**Pin**	**Pin Description**
	1	GND
	2	BLSP8_UART_TX – RS-232 Level
	3	BLSP8_UART_RX – RS-232 Level

14 Customer Designed 4000-OEM Boards and Camera Interface Options

Most common customer configurations integrate the SightLine OEM board designs into a gimbal controller or other boards.

Camera input options are one of the most asked questions about integrating SightLine designs.

All SightLine OEM hardware provides camera input options through SightLine adapter boards to convert camera data into parallel digital video for acquisition. It is often advantageous to integrate both the OEM and the adapter board functionality into the customer hardware.

Customers also integrate an FPGA for switching multiple cameras into a single acquisition interface known as camera switch.

The Sightline EAN-Camera-Switch document is available upon request.

The 4000-OEM provides three options for camera acquisition in a custom designed 4000-OEM board that are described in the next sections.

14.1 Using the Lattice FPGA

The Lattice crosslink FPGA on the 4000-OEM converts parallel digital video into MIPI format data that is captured by the MIPI-CSI2 interface on the SOM. This is similar to using Video Input Port J6 Description (Cam 0).

In this case customers can design in a single camera adapter board or add a separate FPGA on the input to perform camera switch operations. This approach has the advantages of a simple design and assured MIPI format compatibility with the 4000-SOM since the Lattice FPGA does the MIPI generation.

The Lattice FPGA provides tight integration with the 4000-SOM through an I2C register interface. This allows the SOM to reset the FPGA state machine (synchronized to frame sync) by setting a bit in the register interface.

14.2 Not Using the Lattice FPGA

The customer can integrate the camera acquisition, camera switch, and parallel to MIPI conversion in a single FPGA eliminating the need to design in the Lattice crosslink FPGA. This is a more advanced design and is less tightly coupled with the 4000-SOM and adds the complexities of generating MIPI signaling compatible with the 4000-SOM supported formats. This approach may require purchasing a MIPI IP design for the FPGA. See important design details and requirements in EAN-4000-OEM-MIPI-Cameras.

14.3 MIPI Camera Data Acquisition

MIPI format camera data can also be captured directly by the MIPI CSI0 interface on the SOM MIPI Port J9 (Cam 1). For supported MIPI cameras and formats see EAN-4000-OEM-MIPI-Cameras.

15 Questions and Additional Support

For questions and additional support, please contact Support. Additional support documentation and Engineering Application Notes (EANs) can be found on the Documentation page of the SightLine Applications website.