ICD-4100-OEM

2024-06-10

Exports: Export Summary Sheet

EULA: End User License Agreement

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CAUTION: Alerts to a potential hazard that may result in personal injury, or an unsafe practice that causes damage to the equipment if not avoided.

IMPORTANT: Identifies crucial information that is important to setup and configuration procedures.

Used to emphasize points or remind the user of something. Supplementary information aids in the use or understanding of the equipment or subject, which is not critical to system use.

Revision History

Date	Description
2014-05-30	Added 4100-INT Board Custom PCB Options section.
2014-05-21	Updated component temperature range to -40° to 85°C.
2024-05-20	Added finalized dimensional drawing and STEP file.
2024-04-11	Finalize draft. Added preliminary dimensional drawing and STEP file link references.
2024-02-01	Preliminary draft created.

1 Overview

Describes power requirements, thermal management, interface specifications, and connector pinouts for the 4100-OEM video processing board.

CAUTION: Any customer modifications to SightLine OEM and adapter boards will void the warranty and can potentially damage the board. Before attempting any modifications, please contact Support.

1.1 Additional Support Documentation

The Panel Plus User Guide provides a complete overview of settings and dialog windows. Accessed from the Help menu of the Panel Plus application.

The Interface Command and Control (IDD) describes the native communications protocol used by the SightLine Applications product line. It is also available as a PDF from the Software Downloads page.

Additional Engineering Application Notes (EANs) and ICDs are available on the Documentation page.

1.2 Sightline Software Requirements

IMPORTANT: The 4100-OEM requires 3.7.x software and above.

IMPORTANT: The Panel Plus software version should match the firmware version running on the OEM. Firmware and Panel Plus software versions are available on the Software Download page.

2 Safe Device Handling

CAUTION: To prevent damage to hardware boards, disconnect all input power to OEMs and adapter boards before connecting or disconnecting cables including all FFC, FPC, KEL, HDMI, MIPI, and round wire (Molex) cables.

CAUTION: To prevent damage to hardware boards, use a conductive wrist strap attached to a good earth ground. Before picking up an ESD sensitive electronic component, discharge built up static by touching a grounded bare metal surface or approved antistatic mat.

3 4100-OEM Overview

The 4100-OEM consists of a three-board stack: the OEM, INT, and SOM boards. It includes eleven connectors and one microSD card slot. The connectors are used for power, Ethernet, serial ports, MIPI input, HDMI output, USB3, and digital video in (with the use of a 3000-adapter board).

3.1 OEM Serial Number

When contacting Support for OEM board issues it is helpful to provide the serial number. Serial numbers indicate the OEM board type and the license file being used by the board. The serial number on the 4100-OEM is designated with human readable numbers printed on a white label attached to the front of the OEM below the (J6) connector as shown in Figure 1.

3.2 4100-OEM Specifications

Revision: A1
Dimensions: 1.496 in x 1.988 in (38 mm x 50.50 mm)
Weight: Estimate 30 grams
Voltage (VIN): 8 - 15 VDC (12 VDC nom)*
Power: 6 W (For more information on a low power mode to reduce power by 2-4W, see EAN-Performance-and-Latency)
Drawing: 4100-OEM and 4100-INT
STEP File: 4100-OEM STEP and 4100-INT STEP
Rev History: Rev A1: Initial production release.

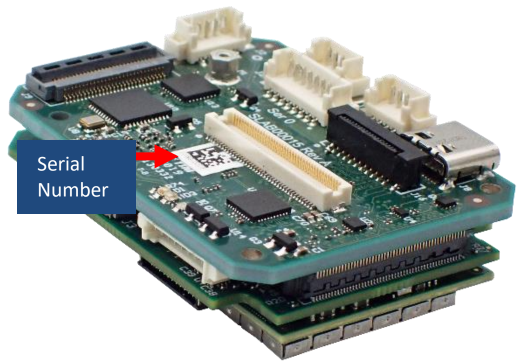


Figure 1: 4100-OEM

**A slightly extended input voltage range is possible with some tradeoffs. Contact Support for more information if this is relevant for a particular application.*

All 4100-OEM board mounting holes support M2 screws 0.086 dia.

3.3 Interface Protocol

The 4100-OEM shares the same interface protocol as other SightLine video processing boards. The protocol is a packet-based command and control interface. The protocol document is available from the SightLine website.

3.4 Functional Block Diagram

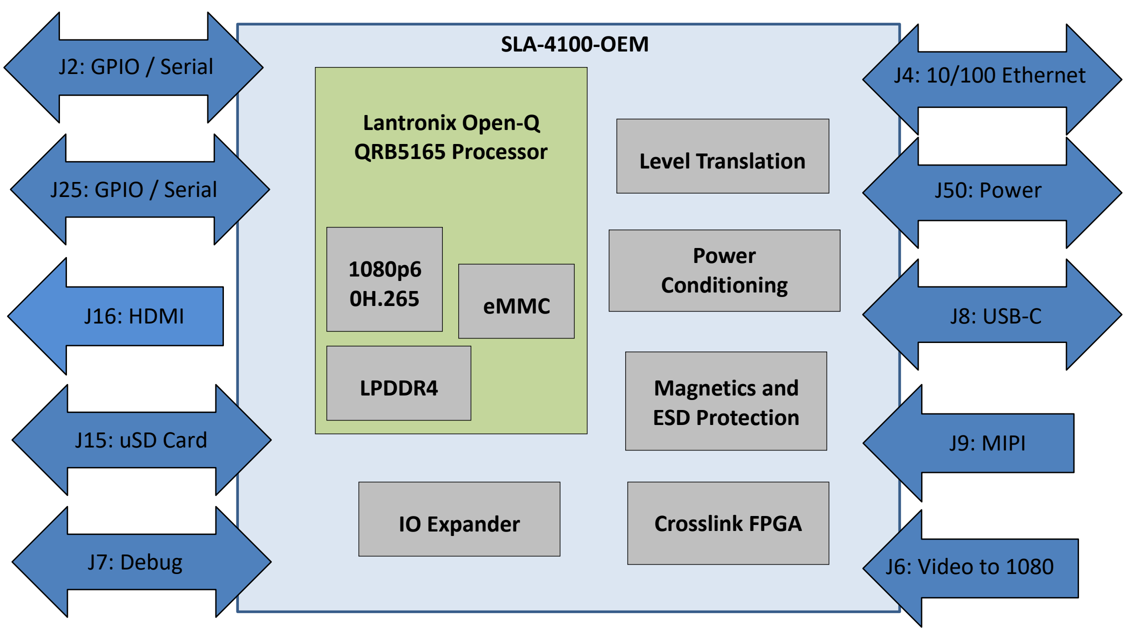


Figure 2: 4100-OEM Functional Block Diagram

3.5 Comms Block Diagram

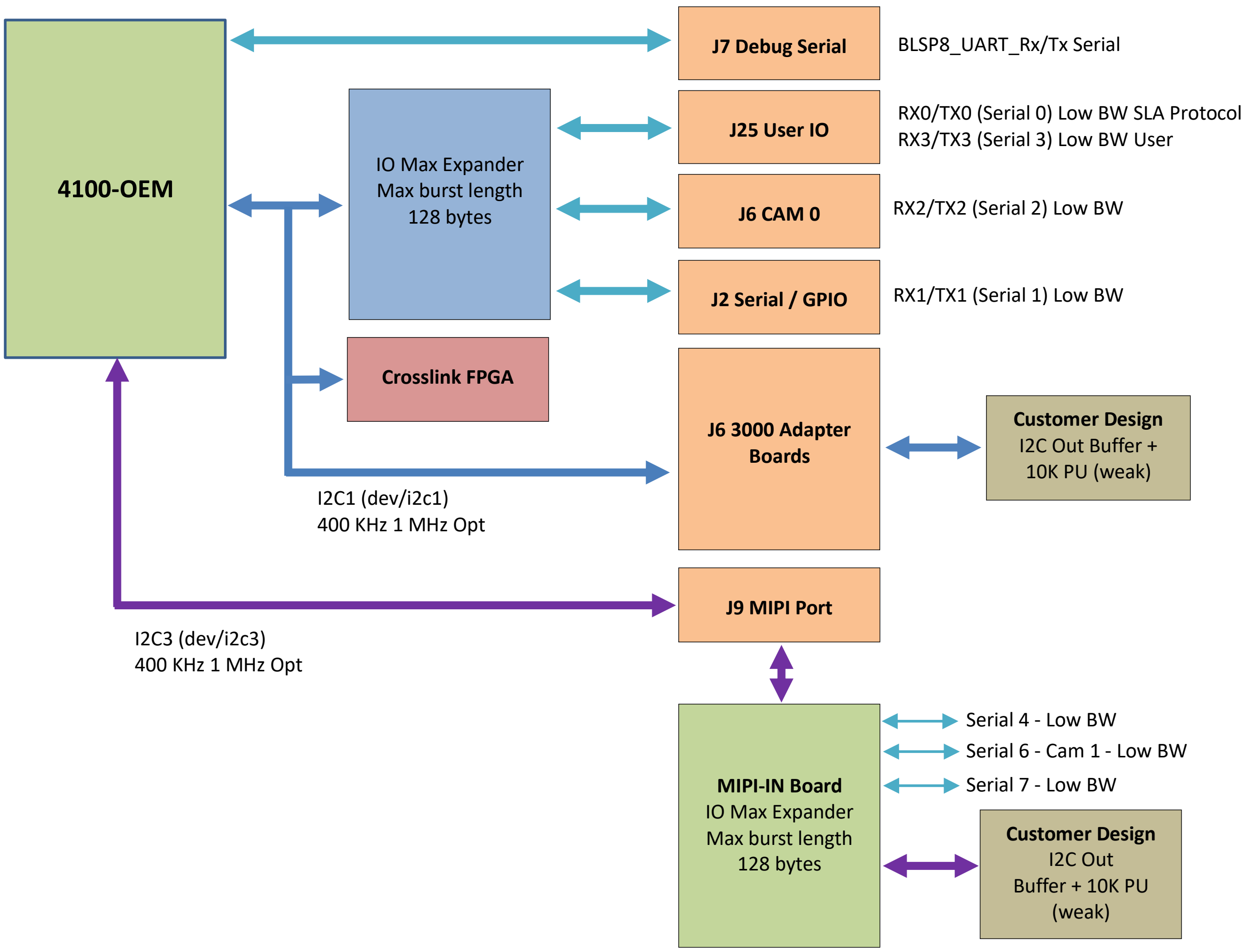


Figure 3: 4100-OEM Comms Block Diagram

3.6 Customer Integration - Key Points

- ✓ Provide a sufficient heat sink for Lantronix Open-Q QRB5165 Processor and other major components. Close attention to heatsinking is critical. See the Thermal Management section for more information.
- ✓ Expose Ethernet port (on J4) to an accessible connector for debug, command and control, and firmware update capability.
- ✓ Expose debug serial port On J7 to an accessible connector for debugging.
- ✓ For in-system recovery, it is recommended to expose the FASTBOOT_RECOVERY switch/button on J7 to a system accessible connector, as well as retain access to the USB port J3 on the 4100-OEM.
- ✓ If you are designing a custom system interface board with the 4100-SOM contact SightLine Support prior to design for assistance.

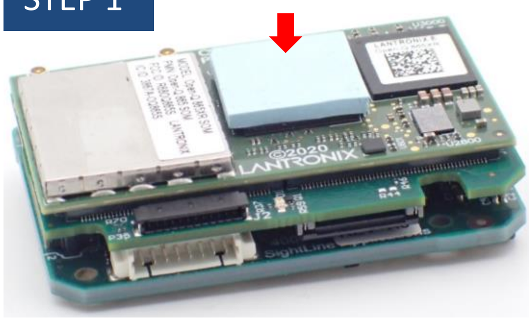
4 4100-OEM Bracket Installation

ⓘ **IMPORTANT:** It is important to install the 4100-OEM on the SLA-4100-BRACKET in the correct orientation. If the bracket is installed backwards, the bracket mounting stanchion can damage the components on the board at R1 and Q1, which will prevent proper power delivery and prevent the unit from booting.

4100-OEM Bracket Kit

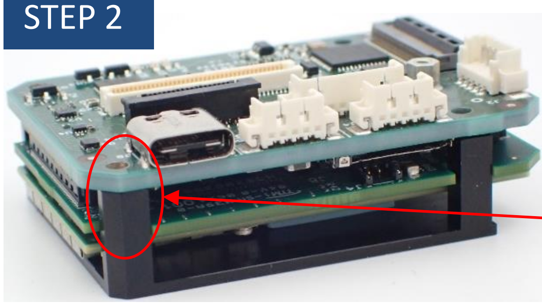
- SLA-4100-BRACKET
- Thermal conductive pad - SLA-PAD-080-01
- 2x SLHW-0035 Mounting Screws
- 2x SLHW-0043 Mounting Screws

STEP 1



Place the thermal conductive pad on the SOM as shown.

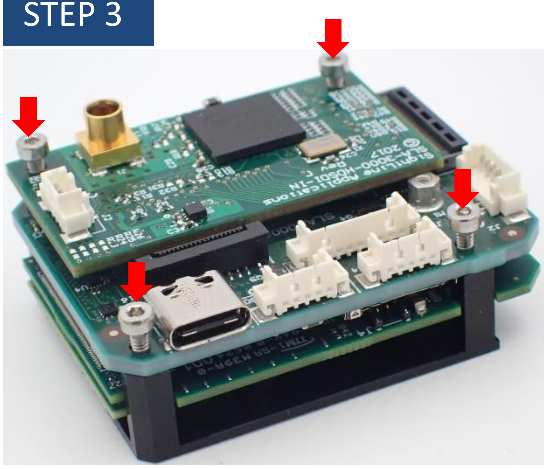
STEP 2



Place the assembled SLA-4100-OEM stack on the SLA-4100-BRACKET it the orientation shown.

ⓘ Pay close attention to the pairing of the chamfered edge. The PCBA chamfer should match the bracket chamfer.

STEP 3



Place the SLHW-0035 and SLHW-0043 into the assembly as shown to fasten the assembly to the mounting surface.

Use SLHW-0001 3mm spacers as needed for adapter board mounting.

Figure 4: 4100-OEM Bracket Installation

5 Thermal Management

5.1 Heatsink Guidelines

IMPORTANT: Close attention to heatsinking is critical.

SightLine screens and certifies all 4100-OEM units through the component temperature range of -40°C to 85°C.

All hardware requires some form of mechanical heatsink.

Customers must design a heatsink in conjunction with their system integration effort. It should provide a direct conducted path to a significant thermal mass (the wall of a gimbal or housing) or use an active cooling (fans) that has proven to be successful in cases where a full thermal analysis is not performed.

The provided SOM cover aids heatsinking when the provided mechanical interface is a flat plate and is our baseline. This cover may be removed, and thermal performance would be improved if a machined heatsink interface is implemented. STEP files for the heatsink interface are available from SightLine that can help with heatsink design and integration.

The 4100-OEM typical power consumption is less than 6W @ 12V. System settings provide an option for a low power mode with no video output but power reduced by 2-4W, see EAN-Performance-and-Latency for more information.

> **CAUTION:** The internal temperature, reported in Panel Plus, should not exceed +85°C (185°F) or the SOM processor will start to reduce clock speed and eventually shut down. Internal high temperatures for extended periods can cause permanent damage.

5.2 Gap Pads

Use some form of thermally conductive material for filling gaps between the hot components and the heat sink. Examples such as the TGlobal TG-A6200 Ultra Soft Thermal Conductive Pad (6W/mK or higher) are recommended. The compression of the pad allows for greater mounting tolerances. The compression of the gap pad also provides additional support for the board and does not require as much force to maintain contact.

5.2.1 Gap Pads SOM Cover

When integrating the OEM with the SOM cover/heat spreader installed (onto a flat surface heatsink), use TGlobal TG-A6200-15-15-2.0 (or Sightline PN: SLA-PAD-080-01), Thermal Pad 1.0 x 1.6 x 0.02 inch.

5.2.2 Gap Pads Without SOM Cover

The cover may be removed if a machined heatsink interface is implemented. STEP files for the OEM with the SOM cover/heat spreader removed are available from SightLine that can help with heatsink design and integration. Contact Support for more information.

6 Connector Descriptions

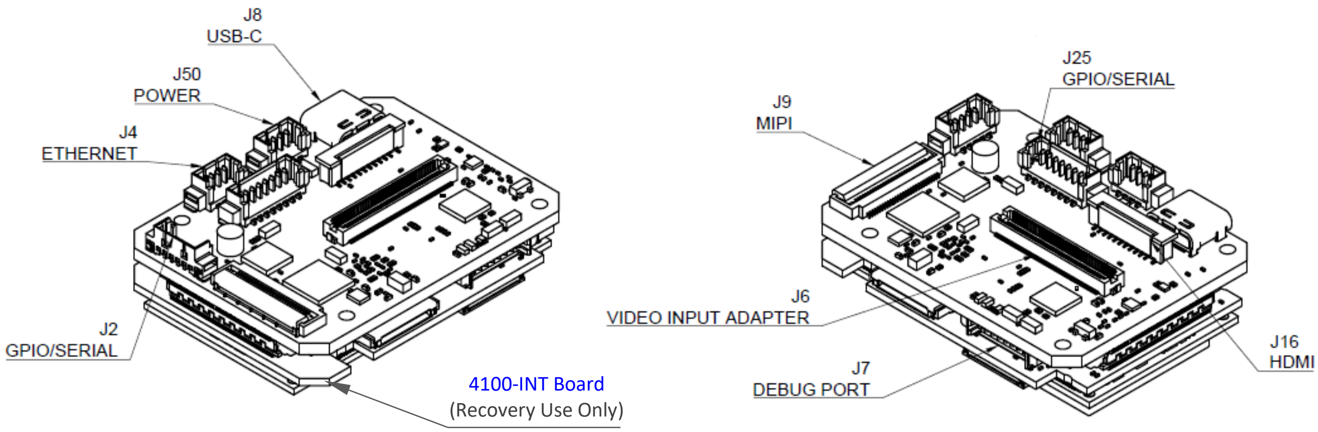


Figure 5: 4100-OEM Connector Descriptions

Table 1: Connector Descriptions

Connector	Description	Mates with:
J2: Serial Port / GPIO	Serial port 1, GPIO	Molex 5POS Housing, 51021-0500
J4: Ethernet 10/100	Ethernet 10/100Mbps	Molex 4POS Housing, 51021-0400
J6: 3000/400 Video Adapter Input	Digital video in 0, serial port 2, I^2C-1, GPIO	DF12(3.0)-80DS-0.5V(86)
J7: 4000-DEBUG / Recovery*	System recovery and debug serial port	Molex 8 POS Housing, 51021-0800
J8: USB 3.0 (Type-C)	USB 3.0 (type C)	USB Type-C Cable
J9: MIPI Port (FFC connector)	MIPI Port, I^2C-3 (Digital Video in 1, serial ports, w/adapter board)	Sightline Cable SLA-CAB-MIPI-02
J15: MicroSD	MicroSD card slot	NA
J16: HDMI Output Video (FFC connector)	HDMI Output (FFC)	Sightline Cable SLA-CAB-HD10
J25: Additional Serial / GPIO	Serial port 0 and 3, GPIO	Molex 8POS Housing, 51021-0800
J50: Power Connector	Typical 12VDC (see 4100-OEM Specifications for min/max)	Molex 4POS Housing, 51021-0400
S2: IO2 SOM	Pinout not included in this ICD. For customers making custom interface boards, contact Support.	NA
S3: IO1 SOM		NA

**The debug serial port is exposed on J7 P7-8 and should be reserved for debugging only. Debug serial port is 1.8V TTL.*

⚠ **CAUTION:** J4 (Ethernet) and J50 (power) are adjacent 4-pin connectors. **DO NOT** connect power to the Ethernet port. Connecting power to the Ethernet port **will** damage the board.

6.1 Connector J2: Serial Port / GPIO

Connector: Molex 5POS, 53398-0571 Mates with: Molex 5POS Housing, 51021-0500

Table 2: Serial Port / GPIO

Pin	Signal	Description
1	GND	
2	TX1	3.3V TTL
3	RX1	3.3V TTL
4	GPIO7	3.3V
5	GPIO8	3.3V

6.2 Connector J4: Ethernet 10/100

Connector: Molex 4POS, 53398-0471 Mates with: Molex 4POS Housing, 51021-0400

Table 3: Ethernet

Pin	Signal	Description
1	TXA_P	TX+
2	TXA_N	TX-
3	TXB_P	RX+
4	TXB_N	RX-

Ethernet supports full duplex.

Supports 10/100BASE-T only.

Ethernet magnetics and Ethernet protection: The 4100-OEM is configured with onboard Ethernet magnetics and ESD protection. It meets the following IEC standards, IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact) IEC 61000-4-4 (EFT) 40A (5/50ns) IEC 61000-4-5 (Lightning) 40A (8/20µs).

6.3 Connector J6: 3000/4100 Video Adapter Input

Connector: DF12(3.0)-80DP-0.5V(86) Mates with: DF12(3.0)-80DS-0.5V(86)

All input signals are assumed to be 3.3V TTL level. Any conversion from a VIOSEL voltage level will be done on the external adapter boards, e.g., SLA-3000-FPC.

Column key for notes column below (data bit locations):

Y = luminance **CbCr** = Chrominance **G** = Grayscale bits.

Table 4: 4100-OEM (J6) Pinout

Pin	Description	Notes	Pin	Description	Notes
2	NC		1	VIN_ACLK	Pixel Clock
4	Ground		3	Ground	
6	VIN_D22		5	VIN_D23	
8	VIN_D20		7	VIN_D21	
10	VIN_D18		9	VIN_D19	
12	VIN_D16		11	VIN_D17	
14	Ground		13	Ground	
16	VIN_D14	**Y**6, **G**14	15	VIN_D15	**Y**7, **G**15
18	VIN_D12	**Y**4, **G**12	17	VIN_D13	**Y**5, **G**13
20	VIN_D10	**Y**2, **G**10	19	VIN_D11	**Y**3, **G**11
22	VIN_D8	**Y**0, **G**8	21	VIN_D9	**Y**1, **G**9
24	Ground		23	Ground	
26	VIN_D6	**CbCr**6, **G**6	25	VIN_D7	**CbCr**7, **G**7
28	VIN_D4	**CbCr**4, **G**4	27	VIN_D5	**CbCr**5, **G**5
30	VIN_D2	**CbCr**2, **G**2	29	VIN_D3	**CbCr**3, **G**3
32	VIN_D0	**CbCr**0, **G**0	31	VIN_D1	**CbCr**1, **G**1
34	Ground		33	Ground	
36	NC		35	NC	
38	NC		37	NC	
40	NC		39	NC	
42	Port ID (out)	See pin notes	41	NC	
44	Ground		43	Ground	
46	NC		45	VIN_HSYNC	Horizontal Sync
48	NC		47	VIN_VSYNC	Vertical Sync
50	NC		49	VIN_FLD	Field
52	NC		51	VIN_DE	Optional

(4100-OEM (J6) Pinout table continued)

54	Ground		53	Ground	
56	Passthrough ground		55	Passthrough VIN	See J50*
58	Passthrough ground		57	Passthrough VIN	See J50*
60	Passthrough ground		59	Passthrough VIN	See J50*
62	Passthrough ground		61	Passthrough VIN	See J50*
64	Ground		63	Ground	
66	TX2	3.3V TTL	65	RX2	3.3V TTL
68	BLSP8_I²C _SDA	I²C-1	67	BLSP8_I²C _SCL	I²C-1 (400 kHz)
70	GPIO1_3000_BRD	3.3V	69	GPIO0_3000_BRD	3.3V
72	GPIO3_3000_BRD	3.3V	71	GPIO2_3000_BRD	3.3V
74	GPIO5_3000_BRD	3.3V	73	GPIO4_3000_BRD	3.3V
76	+3.3V (out)		75	+3.3V (out)	
78	Ground		77	Ground	
80	+1.8V (out)		79	+1.8V (out)	

**Passthrough power available. Max voltage = VIN (See VIN Specifications). Max Current = 1.2A spread across four power and ground pins.*

6.4 Connector J7: 4000-DEBUG / Recovery

A debug serial port is exposed on connector J7 and should be used for debugging only.

Connector: Molex 8 POS, 53398-0871 Mates with: Molex 8 POS Housing, 51021-0800

Table 5: 4000-DEBUG

Pin	Description	Pin	Description
2	Leave Floating	1	Leave Floating
4	uUSB_VBUS	3	GND
6	VOL_N (FASTBOOT_RECOVERY switch)	5	QFIL_USB_SELECT
9	BLSP8_UART_RX (1.8V)	7	BLSP8_UART_TX (1.8)

Debug serial port is 1.8V TTL.

Currently there is not a way to repurpose this port for use by an application on the 4100-OEM. Note that Serial 0 on both the 1500 and 3000 can be repurposed using a silent command. This approach does not work on 4100-OEM hardware.

See the 4000-DEBUG section for more information.

6.5 Connector J8: USB 3.0 (Type-C)

Connector: Molex 1054500101 Mates with: USB Type-C Cable

Table 6: USB 3.0

Pin	Description	Pin	Description
A1	GND	B1	GND
A2	USB3_TX1_N	B2	USB3_TX2_P
A3	USB3_TX1_N	B3	USB3_TX2_N
A4	P5V	B4	P5V
A5	CC1	B5	CC2
A6	USB3_P1_HS1_D_P	B6	NA
A7	USB3_P1_HS1_D_N	B7	NA
A8	NA	B8	NA
A9	P5V	B9	P5V
A10	USB3_RX2_N	B10	USB3_RX1_N
A11	USB3_RX2_P	A11	USB3_RX1_P
A12	GND	A12	GND

USB 5V output can source 900mA max. 5V is also used for MIPI interface boards connected on J9 with a combined maximum of 1.5A.

CAUTION: Do NOT connect an external 5V power source to the USB-C connector. Damage to the OEM may occur.

6.6 Connector J9: MIPI Port (FFC connector)

Connector: Hirose 28POS, FH41-28S-0.5SH (050) Mates with: Sightline Cable SLA-CAB-MIPI-02

The mating cycle rating for this connector is 20 cycles.

Table 7: MIPI Port

Pin	Description	Pin	Description
2	D4+	1	GND
4	GND	3	D4-
6	D3-	5	D3+
8	CLK+	7	GND
10	GND	9	CLK-
12	D2-	11	D2+
14	D1+	13	GND
16	GND	15	D1-
18	IO_HOST_OUT0	17	IO_HOST_OUT1
20	CCIO_I²C_SCL (I²C-3, 400 kHz)	19	GND
22	GND	21	CCIO_I²C _SDA (I²C-3)
24	IO_HOST_IN0	23	IO_HOST_IN1
26	VCC_5V	25	VCC_5V
28	GND	27	VCC_5V

Limit power supplied over FFC cable to 6.75 watts (1.35A @5V).

6.7 Connector J15: MicroSD

Push the microSD into place. To eject it push it again. The socket is rated up to 10,000 mating cycles and has 3.3 mm card eject length.

Recommended microSD card types and previously tested models are discussed in the EAN-File-Recording document.

6.8 Connector J16: HDMI Output Video (FFC connector)

Connector: Amphenol 20POS, 62674-201121ALF Mates with: Sightline Cable SLA-CAB-HD10

Table 8: HDMI

Pin	Description	Pin	Description
2	HDMI_C_5VOUT*	1	HDMI_C_5VOUT*
4	HDMI_C_DATA	3	HDMI_C_HPD
6	HDMI_C_CEC	5	HDMI_C_CLK
8	GND	7	GND
10	HDMI_TMDS_CLK_C_P	9	HDMI_TMDS_CLK_C_N
12	HDMI_TMDS_TX0_C_N	11	GND
14	GND	13	HDMI_TMDS_TX0_C_P
16	HDMI_TMDS_TX1_C_P	15	HDMI_TMDS_TX1_C_N
18	HDMI_TMDS_TX2_C_N	17	GND
20	GND	19	HDMI_TMDS_TX2_C_P

**Not intended for customer use.*

HDMI output:

- Compliant with HDMI v2.0 output.
- See the SLA-HDMI-SDI section in ICD-Adapter-Boards for details on the HDMI to HDSDI converter compatible with this HDMI output.
- FFC Ribbon cable and HDMI connectors: ChenYang Elec.

The HDMI output format is specified by the resolution and format specified through Panel Plus. The HDMI output ignores any EDID HDMI format information in the external HDMI sink device. Supported HDMI formats are defined in SLAVideoDisplay (0xA4) in the IDD.

6.9 Connector J25: Additional Serial / GPIO

Connector: Molex 8POS, 53398-0871 Mates with: Molex 8POS Housing, 51021-0800

Table 9: Extra Serial/GPIO

Pin	Signal	Description
1	GND	
2	TX0	3.3V TTL
3	RX0	3.3V TTL
4	GND	
5	TX3	3.3V TTL
6	RX3	3.3V TTL
7	GPIO6	3.3V
8	GPIO_125	Default MCU_PB3 open drain (Heater control). APQ_GPIO_125 optional w/ resistor load for fan, etc.

6.10 Connector J50: Power Connector

Connector: Molex 4POS, 53398-0471 Mates with: Molex 4POS Housing, 51021-0400

Table 10: J50 - Power Connector

Pin	Description	Description
1	VIN	Typical 12VDC (see Specifications for min/max)
2	VIN	
3	GND	
4	GND	

7 Additional I/O

7.1 LED Summary

Label	**Color**	**Function**
D1	Green	Board Power
D3	Green	IO Expander User LED, GPIO15 (Linux GPIO_467)
D5	Amber	Ethernet PHY Link Indicator

7.2 Serial Ports and USB Serial Ports

All serial ports are 3.3V TTL. When utilizing a SightLine adapter board with a 3-pin connector, use the CAB-03xx cable. This cable facilitates an easy breakout to either a pigtail, Molex-to-Molex, or DB-9 connector.

The USB port on the 4100-OEM can be used for serial communication. A USB hub can be used to create up to three serial ports and can be used to control Cam 2 and Cam 3.

In most cases USB devices will automatically populate as */dev/ttySL** as shown in Table 13. If the camera is not recognized, create a symlink to map a port that can be utilized by VideoTrack, e.g., */dev/ttySL0*. See the *Troubleshooting* section of the EAN USB Video Class UVC Cameras for more information.

Table 11: 4100-OEM Serial Port Summary

Serial Port Name	Notes
Serial Port 0	General purpose (SLA command)
Serial Port 1	General purpose
Serial Port 2	For camera interface use only (Cam 0)
Serial Port 3	General purpose
Serial Port 4	These serial ports are available when attaching an SLA-4000-MIPI board to the MIPI port on J9. See the SLA-4000-MIPI section in the ICD-Adapter Boards. Serial Port 6 is reserved for Cam1.
Serial Port 6	
Serial Port 7	
USB Serial 0	Serial ports exposed through USB. Cameras connected directly to the USB port will usually be exposed through USB Serial 0.
USB Serial 1	
USB Serial 2	

See Connector J7: 4000-DEBUG / Recovery for information on the Debug interface.

Table 12: Serial Ports Hardware Reference - 4100-OEM

Serial 0			Serial 1			Serial 2			Serial 3		
Connector, Pin			Connector, Pin			Connector, Pin			Connector, Pin		
Rx	Tx	level	Rx	Tx	level	Rx	Tx	level	Rx	Tx	level
J25, 3	J25, 2	3.3V	J2, 3	J2, 2	3.3V	J6, 65	J6, 66	3.3V	J25, 6	J25, 5	3.3V

7.2.1 Serial Ports Software Cross Reference

Table 13: Serial Ports Software Cross Reference - 4100-OEM

Connector	Serial Port	Linux Location	Use Cases*	Cam ID
J25	Serial 0	/dev/ttyMAX00	SightLine Video Protocol (SVP) / other protocol types / user defined / other	
J2	Serial 1	/dev/ttyMAX01	User defined / protocol types / other	
J6	Serial 2	/dev/ttyMAX02	Camera control / pass through / protocol types / other	Cam 0
J25	Serial 3	/dev/ttyMAX03	User defined / protocol types / other	
MIPI board	Serial 4,6,7	See the SLA-4000-MIPI section in the ICD-Adapter Boards for details.		
USB	USB Serial 0	/dev/ttySL0	Camera control / pass through / protocol types / other	Cam 2
USB	USB Serial 1	/dev/ttySL1	Camera control / pass through / protocol types / other	Cam 3
USB	USB Serial 2	/dev/ttySL2	Camera control / pass through / protocol types / other	

**See Set Port Configuration for common Protocol Types or EAN-Ethernet-and-Serial-Communication.*

7.2.2 Serial Port Speed and Data Limits

The serial ports are controlled over an I^2C bus using an I^2C to serial bridge chip. The I^2C bus default speed is 400 kHz. The 4100 I^2C bus speed can be changed from the default 400 kHz to 1 MHz.

When increasing the baud rate to 1MHz, care must be taken to ensure that all devices on the bus, including devices located on camera adapter boards, can operate at this speed. See EAN-GPIO-and-I2C for assistance on setting the I^2C bus speed.

Table 14: I^2C and Serial Port Speed Summary

Serial Ports	I^2C Bus	Default Bus Speed
0,1,2,3	i2c-1	400 kHz
4,6,7	i2c-3	400 kHz

⚠ **CAUTION:** The I^2C bus is only shared by a small number of peripherals on the 4100-OEM. Setting I^2C to 1MHz can cause system instability or crashes.

The following Camera I/F boards are known to be incompatible with 1MHz clock:

- SLA-3000-HDSDI (Rev C or older. Rev C1 is compatible)
- SLA-3000-HDMI
- SLA-3000-AB
- SLA-3000-FPC with Airborne camera
- SLA-3000-FPC with SLA-FPC-LI board
- Some custom I/F boards

⚠ **CAUTION:** Some boards are checked by software and will not switch to 1MHz. Other boards cannot be checked by software. It is the responsibility of the user to avoid incompatibilities and resulting system crashes.

7.3 GPIO

The GPIOs on the 4100-OEM are controlled through a MAX14830 chip that supports multiple GPIOs and serial ports. The Linux driver for this chip maps each GPIO pin to a unique GPIO number to allow Linux control of the pin.

The 4100-OEM has ten accessible GPIOs. Six of these GPIOs are routed to the camera input adapter connector J6, while the other four are exposed on round wire connectors J2 and J25.

Four of the six GPIOs that are routed to the adapter board are used by SightLine software to detect the adapter board ID. On some adapter boards the remaining two GPIOs are exposed to round wire connectors for customer use. In rare cases the four GPIOs used to detect the board ID may also be available for customers, though their use is restricted. Contact Support for more information.

All GPIOs on the connectors operate at a voltage of 3.3V, although they can be converted to different voltage domains on the connected adapter boards.

The ICD-Adapter-Boards has a *Camera Input Adapter Board IDs* table, which provides a list of camera input adapter boards and their corresponding IDs. Additionally, the GPIO table in the ICD provides a list of GPIOs that are accessible through round wire connectors on the different camera adapter boards, along with their respective voltage levels.

All GPIO pins have both a schematic name (e.g., GPIO15) and a Linux port name that can be used for control through the operating system (e.g., GPIO_467). GPIO pins are referenced by schematic name and Linux port name, e.g., GPIO15 (Linux GPIO_467).

The Linux port names for these GPIOs are listed in Table 15 for adapter boards connected to the 4100-OEM on J6.

Using the color and letter designator scheme these GPIOs can be cross referenced with the *Customer Accessible GPIOs and Cross Reference* table in the GPIO section of the ICD-Adapter-Boards to match the correct software name to the physical location for GPIOs exposed on SightLine adapter boards.

The voltage level for GPIOs coming off adapter boards is dependent on the adapter board as specified in the ICD-Adapter-Boards.

Table 15: GPIO Software Cross Reference - 4100-OEM

Cross Reference Designator	HW Name (on schematic)	Physical Location (Connector, Pin)	Linux location (in /sys/class/gpio/)
A	GPIO0_3000_BRD	J6, Pin 69	gpio452
B	GPIO1_3000_BRD	J6, Pin 70	gpio453
C	GPIO2_3000_BRD	J6, Pin 71	gpio454
D	GPIO3_3000_BRD	J6, Pin 72	gpio455
E	GPIO4_3000_BRD	J6, Pin 73	gpio456
F	GPIO5_3000_BRD	J6, Pin 74	gpio457
Not routed to adapter boards	GPIO6_USER	J25, Pin 7	gpio458
Not routed to adapter boards	GPIO7_USER	J2, Pin 4	gpio459
Not routed to adapter boards	GPIO8_USER	J2, Pin 5	gpio460

When the SLA-4000-MIPI board is connected to the system, the GPIOs from J10 and J2 on the MIPI board will be mapped to the Linux OS as shown in Table 16. These GPIOs are only available when the MIPI board is connected.

Table 16: GPIO Software Cross Reference - SLA-4000-MIPI

Cross Reference Designator	HW Name (on schematic)	Physical Location (Connector, Pin)	Linux location (in /sys/class/gpio/)
A	GPIO0_3000_BRD	J6, Pin 69	gpio436
B	GPIO1_3000_BRD	J6, Pin 70	gpio437
C	GPIO2_3000_BRD	J6, Pin 71	gpio438
D	GPIO3_3000_BRD	J6, Pin 72	gpio439
E	GPIO4_3000_BRD	J6, Pin 73	gpio440
F	GPIO5_3000_BRD	J6, Pin 74	gpio441
Not routed to adapter boards	GPIO6_USER	J2, Pin 7	gpio442
Not routed to adapter boards	GPIO13_OPEN_DRAIN	J2, Pin 8	gpio449

7.3.1 Advanced GPIO

The 4100-OEM has additional GPIOs that are not exposed on the platform but could be used by customers designing their own carrier boards based on the 4100-OEM design. The GPIO information shown in Table 17 is intended to be used as a starting point for customers designing their own carrier boards and custom applications. They are not intended to be user accessible.

Other GPIOs not shown in this table or other GPIO software reference tables are not available for customer use. Please contact SightLine Support for more information.

Table 17: Advanced GPIO Descriptions - 4100-OEM

Connector, Pin	GPIO port hardware name	Linux location (in/sys/class/gpio/)	Description	Customer Use
J6, P69	GPIO0_3000_BRD	gpio452	Used to detect Board ID	Usable after bootup
J6, P70	GPIO1_3000_BRD	gpio453	Used to detect Board ID	Usable after bootup
J6, P71	GPIO2_3000_BRD	gpio454	Used to detect Board ID	Usable after bootup
J6, P72	GPIO3_3000_BRD	gpio455	Used to detect Board ID	Usable after bootup
J6, P73	GPIO4_3000_BRD	gpio456		Usable after bootup
J6, P74	GPIO5_3000_BRD	gpio457		Usable after bootup
NA	GPIO9_FPGA*	gpio461	FPGA communication with 4100-SOM	Custom board designs
NA	+GPIO10_FPGA*	gpio462	FPGA communication with 4100-SOM	Custom board designs
NA	GPIO11*		Reserved	Not usable
NC	GPIO12*	gpio464	Not Connected	Custom board designs
NA	GPIO13*		Reserved	Not usable
NA	GPIO14*		Reserved	Not usable
NA	GPIO15*	gpio467	LED (Green)	Not recommended
J28, P8	APQ_GPIO_125		Reserved	Not usable

8 Camera Naming Convention

Connector:	**Appears in software as:**
J6 (3000-Adapter board required)	Camera 0 (Cam 0)
J9 (MIPI)	Camera 1 (Cam 1)
J8 USB3 (USB camera)	Camera 2 (Cam 2)

9 Video Input Port J6 Details (Cam 0)

9.1 Adapter boards

When acquiring video, a set of adapter boards are available to convert popular video signals to parallel digital video for input to the J6 video input port. For specific details see ICD-Adapter Boards.

Parallel video can be acquired using an adapter board that accepts FFC and FPC cable types. Mating adapter boards are available that attach to specific camera types (Boson, Airborne, etc.). For more information see the ICD-OEM-Camera-Side-Interfaces *for cable instructions and precautions*.

For custom 4100-OEM board configurations, the information in this section can be used to specify the timing and signals required from the camera interface to the corresponding J6 pin connections. See the Customer Designed 4100-OEM Boards section.

9.2 Camera Power Considerations

- Sony serial digital interface (Sony FCB and Tamron cameras)
- HD-SDI camera interface
- HDMI camera interface
- Camera Link camera interface
- Hitachi camera interface
- Analog video (NTSC and PAL)

ⓘ **IMPORTANT:** The supply voltage level must be compatible with the camera adapter board and connected cameras. For example, the 3000-Sony camera adapter board passes supply voltage directly to the attached camera. A Sony EH series camera can only support 6V - 12V. This would limit the supply voltage to the OEM to this range.

ⓘ **IMPORTANT:** There are multiple rails available on the connectors to power a camera adapter board or accessories. Do not exceed 0.8A on the 3.3V rail. Do not exceed 0.7A on the 1.8V rail.

9.3 Signal Levels and Lattice Crosslink FPGA

Unless otherwise specified, all video signal levels are 3.3 Volts.

The maximum input frequency of the pixel clock is 150MHz. This is limited by the Lattice CrossLink FPGA. The interface bridge is fully programmable, supporting a wide range of video formats, and data rates up to 150 MHz at the CMOS input side.

Pixel data should be valid on the rising edge of the pixel clock.

9.4 Supported Standards

See Table 4 in the Connector J6: 3000/4100 Video Adapter Input section for signal locations.

Additional designations for data bits D0..D15 are included in this table in order to relate these to Grayscale bits (G0..G15) and YCbCr input bits (Y,CbCr).

Unlike the 1500-OEM and 3000-OEM, the 4100-OEM has limitations on the supported resolutions, see the Camera Resolution and Pixel Clock Requirements section.

16-bit YCbCr 4:2:2

- 8-bit luminance acquired in signal locations Y0..Y7
- 8-bit chrominance in signal locations CbCr0..CbCr7
- Progressive video interlaced 1080i supported.

20-bit YCbCr 4:2:2

Use upper 8-bits of 10-bit data for both Y and CbCr.

BT.1120

16-bit BT.1120:

HD 720P and 1080P video

- 8-bit luminance acquired in signal locations Y0..Y7
- 8-bit chrominance in signal locations CbCr0..CbCr7
- Acquisition parameters *Sync/Crop* must be set to *Embedded Sync*

BT.656

Currently only interlaced BT.656 video is supported (PAL or NTSC).

8-bit BT.656:

- Data on signal pins G0..G7 (D0..D7) with pixel clock on VIN_ACLK. See Table 4 in the Connector J6: 3000/4100 Video Adapter Input section. This is different than the 3000-OEM BT.656 connection.

IMPORTANT: For customer designed interfaces based on 3000-OEM adapter boards like the SLA-3000-FPC that support BT.656, the *Byte Swap* checkbox must be selected in the *Acquisition Setting* dialog in Panel Plus. This will swap the input data byte locations since the 3000-OEM board requires BT.656 in the upper 8-bits and the 4100-OEM requires BT.656 in the lower 8-bits.

10-bit BT.656:

- Connect the upper 8-bits of the camera output (10-bits) to the locations shown in Table 4. This will contain the most significant video data, as well as the SAV and EAV codes.

9.5 Grayscale Camera Data

- Up to 16-bit (See Table 4 in the Connector J6: 3000/4100 Video Adapter Input section.)
- 8-bit data in signal locations G0..G7 (G8..G15 should be tied low.)
- 14-bit data in signal locations G0..G13 (G14..G15 should be tied low.)
- 16-bit data in signal locations G0..G15
- Discrete sync signals in signal locations VIN_HSYNC, VIN_VSYNC, VIN_ACLK, VIN_FLD, VIN_DE

9.6 Synchronization Signals

- VIN_VSYNC vertical sync: A rising edge (default) indicates the start of a new frame. This can be configured through acquisition parameters to falling edge.
- VIN_HSYNC horizontal sync: A rising edge (default) indicates the start of a new line. This can be configured through the acquisition parameters to falling edge.
- VIN_ACLK pixel clock: Pixel data is sampled on the rising edge. Maximum input rate is 74.25 MHz. Clock edge is not currently configurable through the acquisition parameters.
- VIN_FLD (not used): The 4000 does not support Field information. MIPI image type does not provide for an Interlaced flag in the MIPI packet header. For BT.656 (analog video) inputs, the 4100-OEM FPGA takes the interlaced data in BT.656 and generates a progressive frame with two fields per frame. It then de-fields these frames during processing. This is not currently supported for other formats, e.g.,1080i is not supported.
- VIN_DE (not used): This is line enable or line valid. Not currently supported on the 4100-OEM.

9.7 Embedded Sync

In this case all synchronization information is in the embedded sync codes - only the pixel clock and the data stream are used.

- BT.1120 (HD, 720/1080P)
- BT.656. (SD – 525/625 lines)

9.8 Camera Resolution and Pixel Clock Requirements

The 4100-OEM Lantronix Open-Q QRB5165 will acquire MIPI and USB format camera data. The camera data format generated by the adapter boards (3000-HDMI, 3000 SDI, etc.) must be converted to MIPI format for acquisition. This conversion is done using a Lattice FPGA, which adds requirements to the pixel clock rate and blanking from the camera.

The following sections help clarify which FPGA version to use for new camera support.

The Lattice MIPI DPhy PLL maximum input clock is 150 MHz. This is different than the specification of the Lattice chip for external clock inputs. See the frequency shown in Table 20 and Table 21 for each version. For additional details on the MIPI interface, clocks, and timing see EAN-MIPI-Cameras. This limits the maximum input pixel clock of the system to 150 MHz.

9.9 Camera Pixel Clock Rate and MIPI Conversion

MIPI is a packetized serial bitstream with a clock rate that is proportional to the camera pixel clock rate. The MIPI clock rate additionally depends on the number of MIPI lanes used (1,2,4) and the bit depth of the camera data.

The SightLine Phase Lock Loop (PLL) in the lattice FPGA generates the correct MIPI clock based on the relevant parameters. This PLL has a limited range of camera pixel clock frequencies that it can lock onto. The lock range is a factor of ~2 on the camera pixel input clock. For example, a PLL generated with a center frequency of 40 MHz will work for camera clock frequencies of approximately 20 to 80 MHz.

Since SightLine supported cameras range from 10 MHz to 150 MHz in input pixel clock frequency, there are several versions of FPGA code to support the varying PLL center frequencies. This PLL center frequency is not dynamically adjustable.

The first FPGA version was generated at 148.5 MHz frequency (1080P60). It will work below 74.25 MHz (1080P30/720P60). After lower frequency FPGA versions were generated, the center frequency was added to the name of the FPGA load.

9.10 Common FPGA Versions

The most common FPGA versions, shown in Table 18, are automatically loaded based on the adapter board ID and the camera resolution/frame rate. Since they are automatically loaded, they do not need to be specified in the *Options* field in the *Acquisition Settings* dialog window in Panel Plus. If they are specified in the *Options* field, they will override the automatically loaded version.

Table 18: FPGA Versions Automatically Loaded for Standard Formats

Camera Format	FPGA Version	MIPI Lanes
720P60, 1080P30,1080P60	GEN_HD	2
NTSC/PAL/BT.656	GEN_SD7208bit	2
640x480/512 8-bit	GEN_640SD8bit	2
640x480/512 16-bit	GEN_640SD16bit	2

For new cameras that do not fit the video timing of standards like 1080P60, the FPGA version can be specified by using the Options field. For example, fpga=GEN_HD.

IMPORTANT: Use the FPGA version with a center frequency closest to the camera pixel clock rate.

For cameras with less than 64 pixels of horizontal blanking, use the FPGA versions shown in Table 20.

Table 19: FPGA Version Names and Pixel Clock Support

FPGA Name	Center Frequency (MHz)	Min Frequency (MHz)	Max Frequency (MHz)	MIPI Lanes
GEN_HD	148.5	74.25	150.00 (FPGA Max)	2
GEN_HD75	74.25	40	Not Tested	2
GEN_HD40	40	20	80	2
GEN_HD20	20	10	40	1

9.11 Horizontal Blanking Requirements

The MIPI data acquired by the 4100-OEM has the following characteristics:

- Each line of video is a separate MIPI packet.
- A packet header is at the start of each packet.
- End-of-frame and start-of-frame packets indicate a full frame of video.

Most video formats provide blanking regions (non-active pixel areas) to help with acquisition. Typically, there are several blanking lines of video at the start of a frame and multiple blanking pixels at the start of each line of video.

The MIPI packet headers are sent during the blanking regions of video. This works for standard HD formats (e.g., 1080P60, 720P60) as there are enough vertical blanking lines and horizontal blanking pixels.

Some custom cameras (mostly IR Cameras) have greatly reduced blanking intervals to increase the frame rates for a specified pixel clock.

In some cases, these blanking intervals are too small to provide enough time to send the additional MIPI overhead.

To use the GEN_HDxx FPGA versions in Table 20 the following criteria is required:

- Two lines of vertical blanking at the start of a video frame.
- 64 pixels or more of total blanking in a single video line. This includes all horizontal timing where pixel values are not active (not visible).

For cameras with less than 64 total horizontal blanking pixels, SightLine has developed versions of the FPGA code that support between 1 and 64 total horizontal blanking pixels.

These versions are designated with an *_F* in the FPGA file name, and use a FIFO to create more blanking area by:

- buffering up the first part of a line of video in a FIFO while outputting the MIPI header packet,
- continuing to buffer in additional input pixel data,
- simultaneously reading data out of the FIFO at an increased output pixel clock rate.

9.12 FPGA Versions for Cameras with Short Blanking Intervals

Table 20 shows the FIFO versions of FPGA that support between 1 and 64 horizontal pixel blanking cameras.

Table 20: FPGA FIFO Version Names for Short Blanking Cameras

FPGA Name	Center Frequency (MHz)	Min Frequency (MHz)	Max Frequency (MHz)	MIPI Lanes
GEN_HD75_F	74.25	40	Not Tested	2
GEN_HD40_F	40	20	80	2
GEN_HD20_F	20	10	40	1

9.12.1 Width and Height Requirements

Both the width and height must be multiples of eight.

9.13 Additional FPGA Versions and naming

Some early versions of the FPGA code only support a fixed width in pixels. These versions have the fixed width in their name.

Table 21: Less Common FPGA Versions

Video format (FPGA Version)	FPGA Name	Width in Pixels	Number Bytes	Pixel Clock MHz	MIPI Lanes
BT.656 (Analog)	GEN_720SD8bit	720	1	27	2
640 (Boson 16 bit)	GEN_HD20	640	2	27	2
640 (Boson 8 bit)	GEN_640SD8bit	640	1	27	2

9.14 Maximum Width and Height

The capture width and capture height are limited to 4112 x 3040. The processed ROI is limited to 4K 3840 x 2160. The ROI can be moved around in the full image by changing the col and row.

10 MIPI Port J9 (Cam 1)

The MIPI port provides an interface directly connecting MIPI cameras to the 4100-OEM. This port provides camera power and camera configuration through I^2C. For details on supported MIPI cameras and formats see EAN-MIPI-Cameras.

The MIPI port can also be used to connect SightLine Video Input adapter boards through the 4000-MIPI adapter board. For details on the 4000-MIPI and Video Input Boards, see the ICD-Adapter-Boards.

11 Camera Input Adapter Board IDs

Each SightLine camera adapter board is assigned a unique adapter ID to simplify setup and configuration. This applies to any board connected to J6 or J9 on the 4100-OEM (J10 on the SLA-4000-MIPI adapter board). See the Camera Input Adapter Board ID table in ICD-Adapter-Boards for a list of camera input adapter boards and IDs.

12 4000-DEBUG

The SLA-4000-DEBUG board provides additional interfacing and software debugging capabilities for the 4100-OEM. It connects to OEM connector J7 and gives the developer access to a debug serial port at RS-232 level, a USB programming/debugging port, and a switch/button combination for board recovery.

Rev A versions of this board are labeled as 4000-RECOVERY. The name was changed after the initial release to 4000-DEBUG. Future revisions will show the new name change.

12.1 Debug Board Specifications

Revision: A2
Dimensions: 1.71 in x 0.96 in (43.4 mm x 24.4 mm)
Weight: 4.5 grams
Voltage: 5V DC, via USB or external power supply
Power < 5 mW
EANs: EAN-OEM-Recovery
Drawing: 4000-DEBUG
STEP File: 4000-DEBUG STEP
Rev History: A: Initial production release

Figure 6: 4000-DEBUG

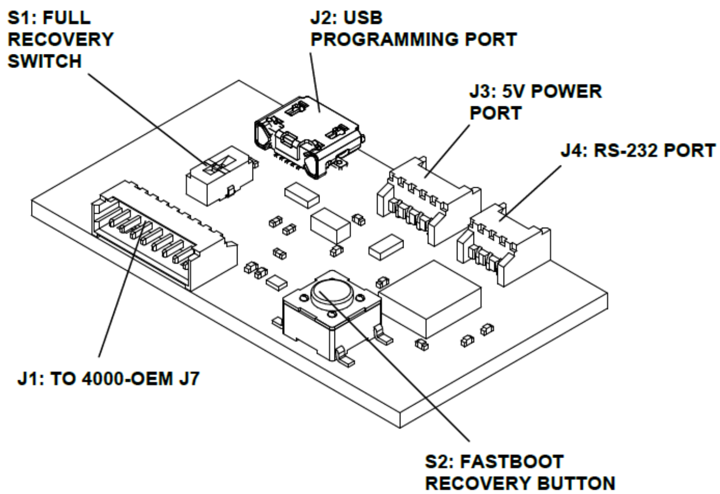


Figure 7: 4000-DEBUG Connector Callouts

Table 22: SLA-4000-DEBUG Board Connector Summary

Label	MFG / MFG Part Number	Function	Mates with:
J1	Molex 53048-0810	To 4100-OEM J7 programming and recovery port	SLA-CAB-XXXX Molex 51021-0800 (housing) and 50058-8000 (terminals)
J2	Amphenol 10118192-0001LF	USB programming port	USB Micro-B to USB-A (PC)
J3	Molex 53048-0410	Power (5 V nominal)	SLA-CAB-1505 Molex 51021-0400 (housing) and 50058-8000 (terminals)
J4	Molex 53048-0310	Serial debug - RS232 level	SLA-CAB-0303 Molex 51021-0300 (housing) and 50058-8000 (terminals)

Table 23: 4000-DEBUG Board Connector Descriptions

Connector	Pin Descriptions	
Connector J1: To 4100-OEM J7 Programming and Recovery port	**Pin**	**Pin Description**
	1	USB3_P0_HS_D_N
	2	USB3_P0_HS_D_P
	3	GND
	4	USB_VBUS (+5V)
	5	FULL_RECOVERY (Switch S1)
	6	FASTBOOT_RECOVERY (Button S2)
	7	BLSP8_UART_TX
	8	BLSP8_UART_RX
Connector J2: USB Programming port	**Pin**	**Pin Description**
	1	USB_VBUS (+5V)
	2	USB3_P0_HS_D_N
	3	USB3_P0_HS_D_P
	4	ID
	5	GND
	6	M1
	7	M2
Connector J3: Power	**Pin**	**Pin Description**
	1	+5V Supply
	2	+5V Supply
	3	GND
	4	GND
Connector J4: Serial Debug Port	**Pin**	**Pin Description**
	1	GND
	2	BLSP8_UART_TX – RS-232 Level
	3	BLSP8_UART_RX – RS-232 Level

13 Customer Designed 4100-OEM Boards and Camera Interface Options

Most common customer configurations integrate the SightLine OEM board designs into a gimbal controller or other boards.

All SightLine OEM hardware provides camera input options through SightLine adapter boards to convert camera data into parallel digital video for acquisition. It is often beneficial to integrate both the OEM and the adapter board functionality into customer hardware.

The 4100-OEM provides several options for camera acquisition in a custom designed 4100-OEM board that are described in the next sections.

13.1 Using the Lattice FPGA

The Lattice crosslink FPGA on the 4100-OEM converts parallel digital video into MIPI format data that is captured by the MIPI-CSI2 interface on the SOM.

Connector:	Appears in software as:
J6 (3000-Adapter board required)	Camera 0 (Cam 0)
J9 (MIPI)	Camera 1 (Cam 1)
J8 USB3 (USB camera)	Camera 2 (Cam 2)

In this case, customers have the option to either design a single camera adapter board or add a separate FPGA on the input for performing camera switch operations. This approach offers the advantages of a simple design and guaranteed compatibility with the 4100-SOM in terms of the MIPI format, as the Lattice FPGA handles the MIPI generation.

The Lattice FPGA provides tight integration with the 4100-SOM through an I^2C register interface. This allows the SOM to reset the FPGA state machine (synchronized to frame sync) by setting a bit in the register interface.

13.2 Not Using the Lattice FPGA

The customer can integrate the camera acquisition, camera switch, and parallel to MIPI conversion in a single FPGA eliminating the need to design in the Lattice crosslink FPGA. This is a more advanced design and is less tightly coupled with the 4100-SOM and adds the complexities of generating MIPI signaling compatible with the 4100-SOM supported formats. This approach may require purchasing a MIPI IP design for the FPGA. See important design details and requirements in EAN-MIPI-Cameras.

13.3 MIPI Camera Data Acquisition

MIPI format camera data can also be captured directly by the MIPI CSI0 interface on the SOM MIPI Port J9 (Cam 1). For supported MIPI cameras and formats see EAN-MIPI-Cameras.

13.4 4100-INT Custom PCB Options

Customers have two primary options for integrating the 4100-INT board into a custom PCB:

- **Option 1:** The customer designs a custom PCB that includes all the electronics from both the 4000-OEM and the 4100-INT. The 4100-SOM from SightLine can then be purchased and placed on the PCB.
- **Option 2:** The customer designs a custom PCB that includes only the electronics from the 4000-OEM and then purchases both the 4100-SOM and the 4100-INT PCBA from SightLine.

In both cases, customers can utilize the newer OEM SOM. This flexibility allows customers to select the configuration that best meets their needs.

14 Questions and Additional Support

For questions and additional support, please contact SightLine Support. Additional support documentation and Engineering Application Notes (EANs) can be found on the Documentation page of the SightLine Applications website.